NuBus Graphics Card Theory of Operations

Toby Farrand
Advanced Development Group
Computer Graphics Lab
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Updates to the Specification

- This specification applies only to the DVT version of the NGC labeled 1.0.
- The CLUT register spaces have moved.
- No reads of the card's control of status bits are supported.
- The configuration ROM is now 1K bytes.
- A section on debugging of the card has been added.

Table of Contents

1.0 Overview

The NuBus Graphics Card (NGC) is a high performance, flexible and low cost color graphics card for any Apple NuBus based product. The card is based on the TFB frame buffer controller chip designed in the Advanced Development Group, and is targeted for introduction with the Milwaukee machine.

1.1 Features

The NGC features variable color depth operation of either 1,2,4 or 8 bits per pixel with a color lookup table providing a palette of 16M colors driving 8 bit DACs for each of the RGB channels.

The card is capable of generating proper timing for the Milwaukee monitors, or any RS170 compatible monitor. (This includes such things as analog film recorders and projection TVs.)

The board features high performance -- 400ns reads and writes from the NuBus interface.

1.2 Cost

The board is expected to cost no more than $110 for the 512K byte version capable of supporting up to 8 bits per pixel color. A cost breakdown is given below:

ITEM	APPLE PART NUMBER	PART DESCRIPTION	QUANTITY PER BOARD	EST. UNIT COST	PART COST PER BOARD
1		TFB (Apple Custom)	1	14.50	14.50
2		NEC video RAM µPD41264 150ns	16	3.00	48.00
3		PAL16R4B 15ns PAL	1	1.75	1.75
4		PAL 20R6A 25ns PAL	1	1.75	1.75
5		Brooktree Bt453 CLUT/DAC Chip	1	12.00	12.00
6		2716 16K EPROM	1	0.75	0.75
7		74F153 Dual 4:1 MUX	1	0.90	0.90
8		AM29841 Ten Bit Latch	1	0.90	0.90
9		74F521 Octal Comparator	1	1.00	1.00
10		74F245 Octal Buffer	4	0.55	2.20
11		74F00 QUAD NAND Gate	1	0.20	0.20
12		74F38 QUAD NAND Gate	1	0.25	0.25
13		HY5030-100 Tapped Delay Line	1	2.50	2.50
14		12.2727 MHz Oscillator	1	1.30	1.30
15		30.2400 MHz Oscillator	1	1.80	1.80
16		96 Pin NuBus Connector	1	2.30	2.30
17		D-Shell 15 pin connector	1	1.75	1.75
18		LM385-1.2 Voltage Reference	1	0.20	0.20
19		.1µF Decoupling Capacitor	30	0.03	0.90
20		10µF Bulk Capacitor	5	0.20	1.00
21		Ferrite Bead	2	0.12	0.24
22		Resistor SIP Pack 10 pin 22 ohm	4	0.10	0.40
23		Resistor, 3.3K ohm 5%	1	0.01	0.01
24		Resistor, 47K ohm 5%	1	0.01	0.01
25		Resistor, 75 ohm 5%	3	0.01	0.03
26		PC Board, 4 layer 4" X 13"	52	0.19	10.00
		TOTAL for 1,2 or 4 Bit Card			82.64
		TOTAL for 1,2,4 or 8 Bit Card			106.64

Note that a 256K byte configuration supporting 256K bytes of video memory would cost less than $85. Many of the costs given above are estimates, actual numbers are likely to vary.

2.0 Software Interface

In addition to the 256K to 512K of video memory which QuickDraw manages, most of the features on the NGC are subject to software control through several control address spaces. All of the address spaces are located in the 16Mbyte "slot space" documented in the NuBus specification.

2.1 Memory Map

A memory map of the 16Mbyte "slot space" is given below:

A19	A18	A17	A16	A3	A2	Selected Space
0	X	X	X	X	X	RAM Space (8 Mbytes)
1	0	0	0	X	X	TFB Control Space
1	0	0	1	X	X	Color Table
1	0	1	0	X	X	Clear Vertical Interrupt
1	0	1	1	X	X	Set Interlace Bit
1	1	0	0	X	X	Clear Interlace Bit
1	1	0	1	0	0	*Read VSYNC~ State
1	1	0	1	0	1	*Read Vertical Interrupt State
1	1	0	1	1	0	*Read Interlace Bit
1	1	1	0	X	X	Unused
1	1	1	1	X	X	ROM

* These options are not supported on the DVT card. Only the read VSYNC~ option is likely to be supported on the final card.

RAM Space

Only the first 256K or 512K bytes of the RAM space are used. Note that all of the address spaces take up just 1MB of the NuBus slot space. This makes the board compatible with the Milwaukee "24 bit mode."

TFB Control Space

This is where the 16 8-bit control registers in the TFB are located. The TFB values for the cards's various modes of operation are given in section **2.2 TFB Operation.**

Color Table

The NGC uses the Bt453 integrated lookup table and DAC chip from Brooktree. Refer to the Bt453 data sheet for details of its operation. Apple is actively pursuing alternate vendors for this part. The code below shows how the CLUT could be initialized with a linear ramp:

```
SetCLUT     PROC   EXPORT
            move.b #$FF,d0
            move.l #CardBase+CLUTAddReg,a0
            move.b d0,(a0)
            move.l #CardBase+CLUTDataReg,a0
            move.l #$FF,d0
@1          move.b d0,(a0)
```

```
move.b d0,(a0)
move.b d0,(a0)
dbra   d0,@1
rts
```

Clear Vertical Interrupt

The NGC uses the "dumb" interrupt mechanism on the NuBus to indicate the beginning of the vertical blanking period. This interrupt is cleared by any access to this address space.

Set Interlace Bit

The NGC has two oscillators which it can use as a pixel clock -- a 30.24 MHz oscillator for the Milwaukee monitors, and a 12.2727 MHz oscillator for generating RS170 timing video. An access to this address space will cause the 12.2727 MHz oscillator to be selected. The interlace bit is cleared with any RESET of the machine.

Clear Interlace Bit

An access to this address space will select the 30.24 MHz oscillator as the pixel clock. The state of the interlace bit should only be changed when the TFB is in a soft reset mode (Refer to the TFB specification for details.)

Read VSYNC~ State *

When a read to this address space is made, the current state of the VSYNC~ signal is placed on the D24 bit of the NuBus. Note that the VSYNC~ signal is valid only for a few lines at the very start of the vertical blanking period.

Read Vertical Interrupt State *

When a read to this address space is made, the current state of the vertical interrupt signal is placed on the D24 bit of the NuBus.

Read Interlace Bit *

When a read to this address space is made, the current state of the interlace bit is placed on the D24 bit of the NuBus.

ROM

The configuration ROM is located at every 4th address in the high 4096 bytes of the "slot space".

2.2 TFB Operation

The operation of the TFB is described in the TFB specification document which is available from Toby Farrand at MS 22Y. The next two sections describe how the TFB must be set up to provide the 8 different video modes supported by the NGC, and the procedures for setting up the TFB.

2.2.1 TFB Register Values

Aside from the interlace control bit described above, all of the video modes available on the NGC are controlled by the control registers on the TFB. The following table gives the values to be placed in the TFB in order to get the various modes of operation. The TFB values are written to

every fourth address starting at $00X80000 where X indicates the slot number of the NGC.

Register Data

NGC Configuration	$X80000	$X80004	$X80008	$X8000C	$X80010	$X80014	$X80018	$X8001C	$X80020	$X80024	$X80028	$X8002C	$X80030	$X80034	$X80038	$X8003C
1 Bit Per Pixel Non-Interlace	$20	$47	$00	$00	$1E	$E5	$77	$46	$05	$02	$02	$01	$0F	$41	$05	$C8
2 Bit Per Pixel Non-Interlace	$40	$47	$00	$00	$3C	$E5	$77	$46	$05	$06	$06	$04	$20	$04	$0B	$D8
4 Bit Per Pixel Non-Interlace	$80	$47	$00	$00	$78	$E5	$77	$46	$05	$0E	$0E	$0A	$42	$8A	$16	$E8
8 Bit Per Pixel Non-Interlace	$00	$47	$00	$00	$F0	$E5	$77	$46	$05	$1E	$1E	$16	$86	$96	$2D	$F9
1 Bit Per Pixel Interlace	$20	$B7	$00	$00	$16	$E5	$3B	$19	$05	$00	$00	$00	$10	$00	$05	$C8
2 Bit Per Pixel Interlace	$40	$B7	$00	$00	$2C	$E5	$3B	$19	$05	$02	$04	$02	$22	$02	$0B	$D8
4 Bit Per Pixel Interlace	$80	$B7	$00	$00	$58	$E5	$3B	$19	$05	$03	$0C	$06	$42	$06	$17	$E8
8 Bit Per Pixel Interlace	$00	$B7	$00	$00	$60	$E5	$3B	$19	$05	$08	$1A	$0E	$86	$9E	$2E	$F9

TFB Register Values for the 8 Possible NGC Modes of Operation

To change the depth of the pixel data being generated, or to change the timing to RS170 or Milwaukee timing, the values above should be sent to the NGC. The following code sequence shows how this can be done:

```
SetTFBDepth   PROC   EXPORT
              move.l #CardBase+TFBBase,A1
              move.w 4(A7),D0       ;D0 tells the depth
              sub    #1,D0
              lea    BPP1N,A0       ;get the address of the TFB values
              move.l A0,D1
              lsl.l  #4,D0          ;desired values are at BPP1N+16*depth
              add.l  D0,D1
              move.l D1,A0          ;A0 points to desired TFB values
              move.b #$B7,$3C(A1)   ;Put the TFB into a reset state
              move.l #15,D0         ;Fill 16 TFB registers
@1            move.b (A0)+,D2       ;move a byte
              not.l  D2
              move.b D2,(A1)
```

```
            move.l A1,D1
            addq.l #4,D1
            move.l D1,A1
            dbra   D0,@1          ;do it 16 times
            rts

;     Invert these values before begin used since the NuBus is an inverted
;     bus

BPP1N  DC.B   $20,$47,$00,$00,$1E,$E5,$77,$46,$05,$02,$02,$01,$0F,$41,$05,$C8
BPP2N  DC.B   $40,$47,$00,$00,$3C,$E5,$77,$46,$05,$06,$06,$04,$20,$04,$0B,$D8
BPP4N  DC.B   $80,$47,$00,$00,$78,$E5,$77,$46,$05,$0E,$0E,$0A,$42,$8A,$16,$E8
BPP8N  DC.B   $00,$47,$00,$00,$F0,$E5,$77,$46,$05,$1E,$1E,$16,$86,$96,$2D,$F9

            ENDP
```

Eventually, some care should be taken to be sure that the TFB is reset, initialized, and set to go again in a synchronous manner with respect to the vertical sync pulse. This will prevent the screen from jumping each time the depth is changed.

2.2.2 TFB Initialization

When the system is reset, the TFB should be assumed to be in a state in which no video timing pulses or RAM refresh is taking place. Furthermore, the TFB is assumed to be in a state where it is not prepared to do a normal NuBus access. This is because a hard reset forced the TFB into behaving as if it were talking to a 68020 rather than a NuBus interface. To initialize the TFB into 1 bit per pixel mode, the following code sequence should be run. This sequence should be run only after a reset has occurred:

```
SetUpTFB    PROC   EXPORT
            move.l #CardBase+TFBIBase,A0    ;get the card's base address
            lea    reg0,A1                  ;point to the data block
            move.l #15,D0              ;loop 16 times
@1          move.b (A1)+,(A0)
            move.l A0,D1
            sub.l  #4,D1
            move.l D1,A0
            dbra   D0,@1
            rts                        ;return

;     The following data constants are used for 1 bit per pixel,
;     non-interlaced 640X480 at 30,24MHz operation

Reg0   DC.B   $DF,$B8,$FF,$FF,$E1,$1A,$88,$B9,$FA,$FD,$FD,$FE,$F0,$BE,$FA
RegF   DC.B   $37          ;3F turns off NuBus
                           ;37 turns on NuBus
            ENDP
```

Note that this code assumes the graphics card to be in slot 1 in the Milwaukee.

3.0 Hardware Description

The NGC hardware design is fairly straight forward since all of the RAM and video timing, and video generation is performed by the TFB. The design has four main blocks:

- NuBus Interface
- Timing Generator
- Frame Buffer
- Video Output

Each of these blocks is described below. Refer to the schematics to aid understanding of the description.

3.1 NuBus Interface

The interface to the NuBus is fairly straight forward. The AD lines from the bus are buffered via 74F245 bus tranceivers. Ten address bits are latched for use in addressing the ROM and the CLUT control registers. The awkward byte ordering of the NuBus versus the 680x0 is handled at the frame buffer, the control spaces put data on byte lane 0 of the NuBus.

3.2 Timing Generation

The timing generation circuitry performs three main tasks. It generates the signals necessary for interfacing to the TFB, it generates the handshake and control signals for the NuBus, and it generates control signals for the various control spaces on the NGC.

The TFB interface involves the generation of three signals.

The PAS~ signal acts as an address strobe to for the TFB. NuBus addresses are latched on the TFB on the falling edge of PAS~. PAS~ remains asserted until the ACK~ signal is returned to the NuBus master. The TFB will not initiate a RAM access unless PAS~ is asserted.

The RAMSEL~ signal indicates that a RAM access is to be initiated on the following NuBus clock. This signal acts to synchronize the TFB to the NuBus. The TFB will initiate a RAM access any time both PAS~ and RAMSEL~ are asserted and there is no RAM refresh cycle in progress.

Finally, since the TFB expects to run from twice the bus clock, there is a 100ns tapped delay line used to generate a 20 MHz signal from the NuBus 10 MHz clock. The 25% duty cycle of the NuBus clock makes generating a 20 MHz clock fairly simple.

The NuBus handshake and control signals are generated from a state machine found in the PAL at U5F.

There are three types of bus cycles which the NGC may execute:

- A RAM write cycle.
- A RAM read cycle.
- A control space cycle.

The decode for the various control spaces on the NGC is performed by the PAL at U4E. The equations for the three PALs are given at the end of this document. The basic timing for the RAM and control space accesses is also given at the end of the document.

3.3 Frame Buffer

The TFB performs almost all of the functions necessary for controlling the RAM, refreshing the RAM and generating video data and timing. The RAM control signals need not be buffered, 47

ohm resistors are used to damp the RAM control signals. Notice that the TFB has both a pixel clock input and output. This is done to ease the timing requirements of the video generation circuitry.

3.4 Video Output

The video output stage begins with generating the desired pixel clock. The schematics show three possible sources of the TFB pixel clock. Only two are likely to be used in actual operation.

The interlace signal selects between the RS170 pixel clock and the Milwaukee monitor pixel clock. If Pixel Bus is being used, then it will generated a PBCLK_SEL signal which selects the EXT_PBCLK. This will only be used in ADG and so is not of general interest.

The selected pixel clock, now called TFB_CLK is sent to the TFB. The TFB generates its own version of the pixel clock which is buffered (PX_CLK) and sent to the rest of the pixel generation circuit.

Care should be taken in the placement and route of the CLUT chip and J2 in order to reduce parasitic effects on the analog RGB signals.

4.0 Schedule

Prototype NGC1.0 boards are up and running.

1000 TFB controllers will be here in a couple of weeks, a turn of the TFB is underway with both LSI Logic and Toshiba. We are looking into plastic flat pack package for the TFB.

The Bt453 is being sourced by Fairchild, Brooktree will be able to handle our first half 1987 needs.

5.0 Debugging

No cuts or jumps are required for the NGC1.0 boards. The debugging procedure is as follows:

- Stuff the board, socket components at U4B, U4E, U5F and U7B, U8F.

  Boards are to be stuffed by an outside company so stuffing of the socketed components is probably the only task here. Take care to stuff the TFB with pin A1 in the lower left. Don't stuff the ROM at U8F for now. Make sure you have the latest PAL versions for U4E and U5F.

- Check the board for power to ground shorts.

  Beep any power and ground connections for shorts.

- Plug board in Milwaukee slot 1. Milwuakee should have "old" video card in slot 6.

  Initially, you will not boot from the board under test.

- Plug monochrome monitor into "old" video card, plug color monitor into board under test.

  No need to waste a color monitor where a monochrome will do.

- Boot Milwaukee.

If the Milwaukee doesn't boot then the board may have a:

- Shorted an address/data line at J1.
- Bad connection related to the NuBus control signals at U6E and U5F.
- Almost anything on the board relating to the NuBus interface could be failing.

- Run the NGC Diags program.

  This program is designed to work with the NGC under test in slot 1. It has options to initialize the TFB, run memory tests, change the CLUT, set the frame buffer depth etc.

- Select "Init CLUT" menu option.

  This option initializes the CLUT on the board.

- Select "Init TFB" menu option.

  This option sets up the TFB for 1 bit per pixel operation. A dim random display should appear on the color monitor. If nothing appears then:

  - The TFB wasn't initialized, something may be wrong around U4E or U5F.
  - Try running a memory test, the frame buffer my be blank.
  - Check pin 21 of U7B. If it is static, then the TFB was definitely unititialized, if it is toggling, then check the pixel data lines coming into U7B.

  If vertical lines appear on the screen:

  - The board may have a stuck video data bit coming off the RAM.
  - The board may have a stuck data bit coming off the bus. Run a memory test to see if your RAM is good.

  If the screen is anything but black and white, then the CLUT is not being initialized properly.

- Run memory tests.

  We have yet to find a bad RAM chip. If you get memory errors, it is probably a stuck address or data line.

6.0 Final Board Features

The final board feature set varies from the DVT board in only a few respects:

- The ability to read the state of the VSYNC~ line will be supported.
- Up to 4K bytes of configuration ROM will be supported.

7.0 Layout

A plot of the layout is attached.

Note that the power and ground planes are split into two segments. The segments are connected via a ferrite bead at L1 and a 1/2 inch ground plane connection near L1. A 1/8th inch spacing is necessary between the separate VCC and GND planes. Components labeled

C2-C6,R4-R7,D1,U22 and J2reside on the AGND and AVCC planes. Additionally, the RED, GREEN and BLUE signals should not reside on the AVCC plane (this is to improve power supply rejection on these analog signals.) All capacitors and resistors residing on the AGND plane should be placed as close as possible to U22.

8.0 Bt453 Specification

Attached.

9.0 Schematics

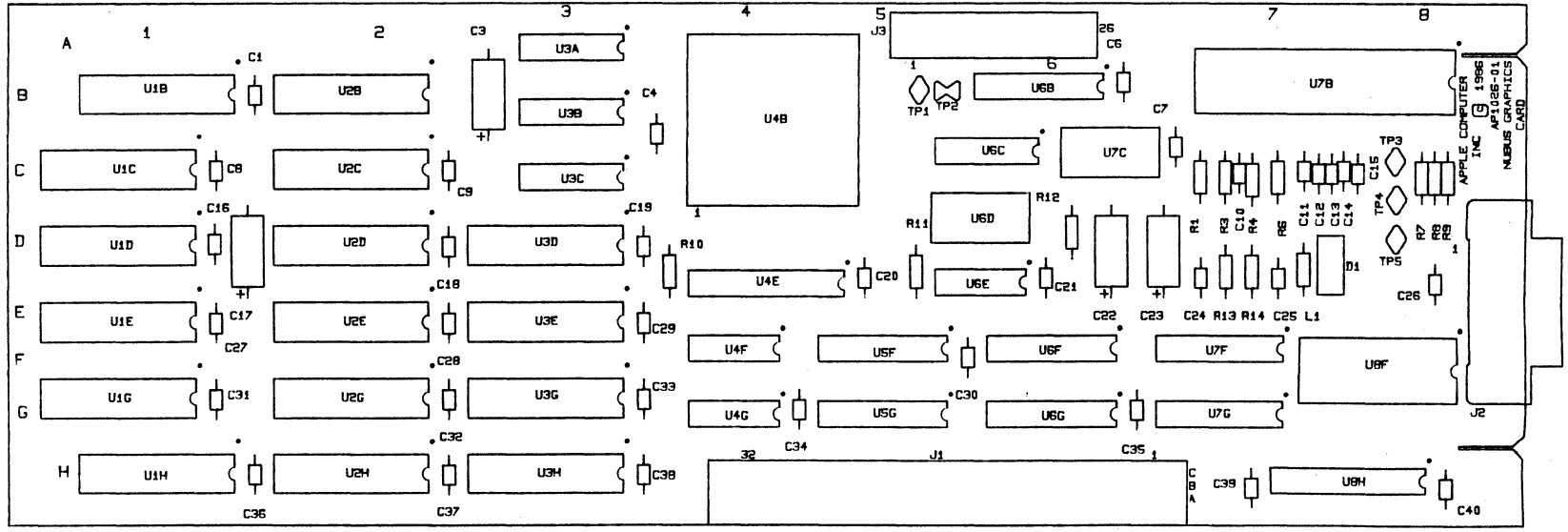
Attached.

10.0 PAL Equations

Attached.

11.0 Timing Diagrams

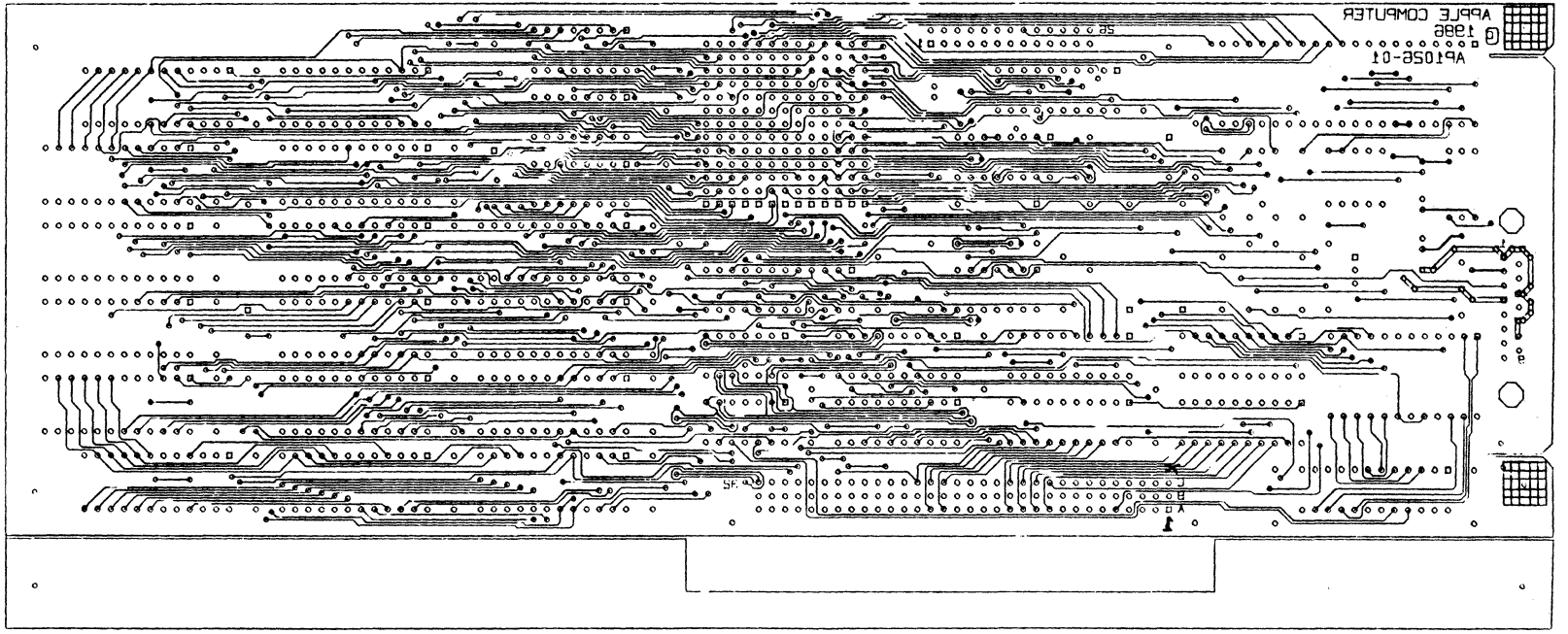
Attached.



J1C
J1B
J1A

PCB, NUBUS GRAPHICS CARD
AP1026-01
SILKSCREEN

ACCUTEK C016 12-JULY-86 DE



PCB, NUBUS GRAPHICS CARD
AP1026-01
NON-COMPONENT SIDE, LAYER 4

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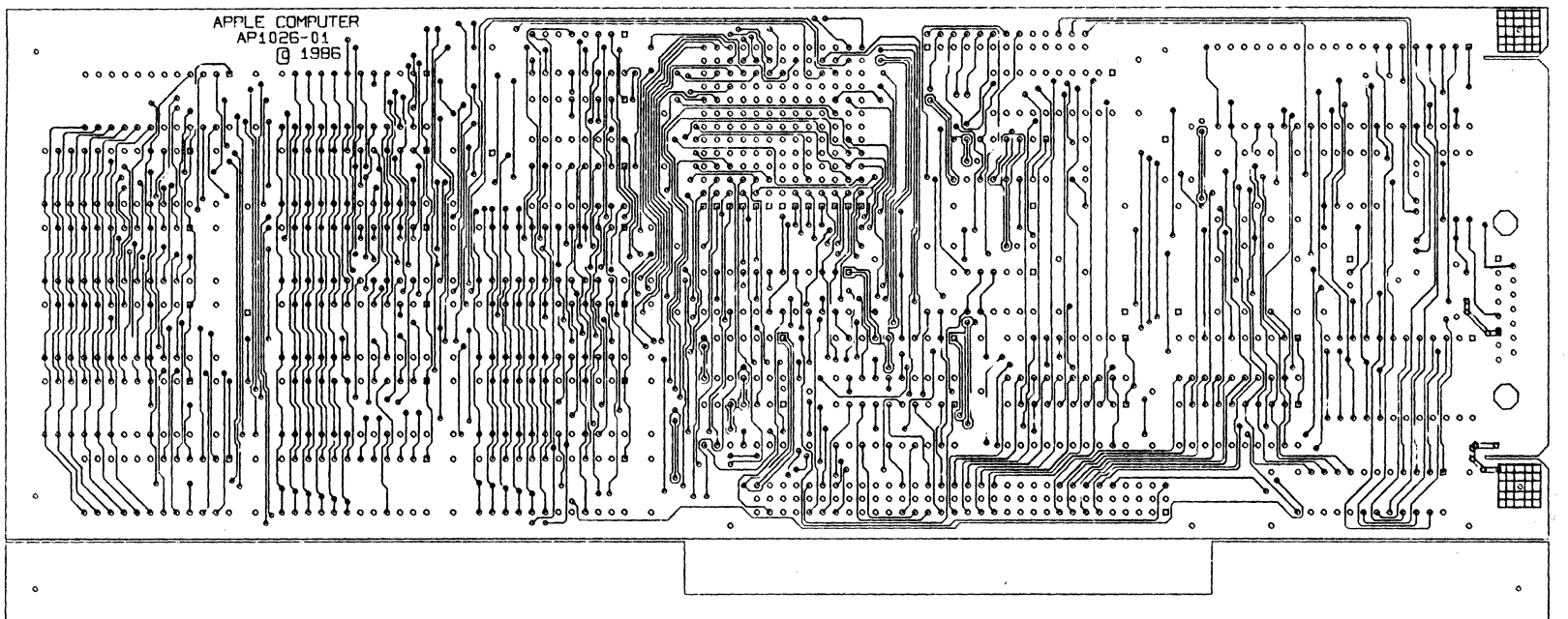

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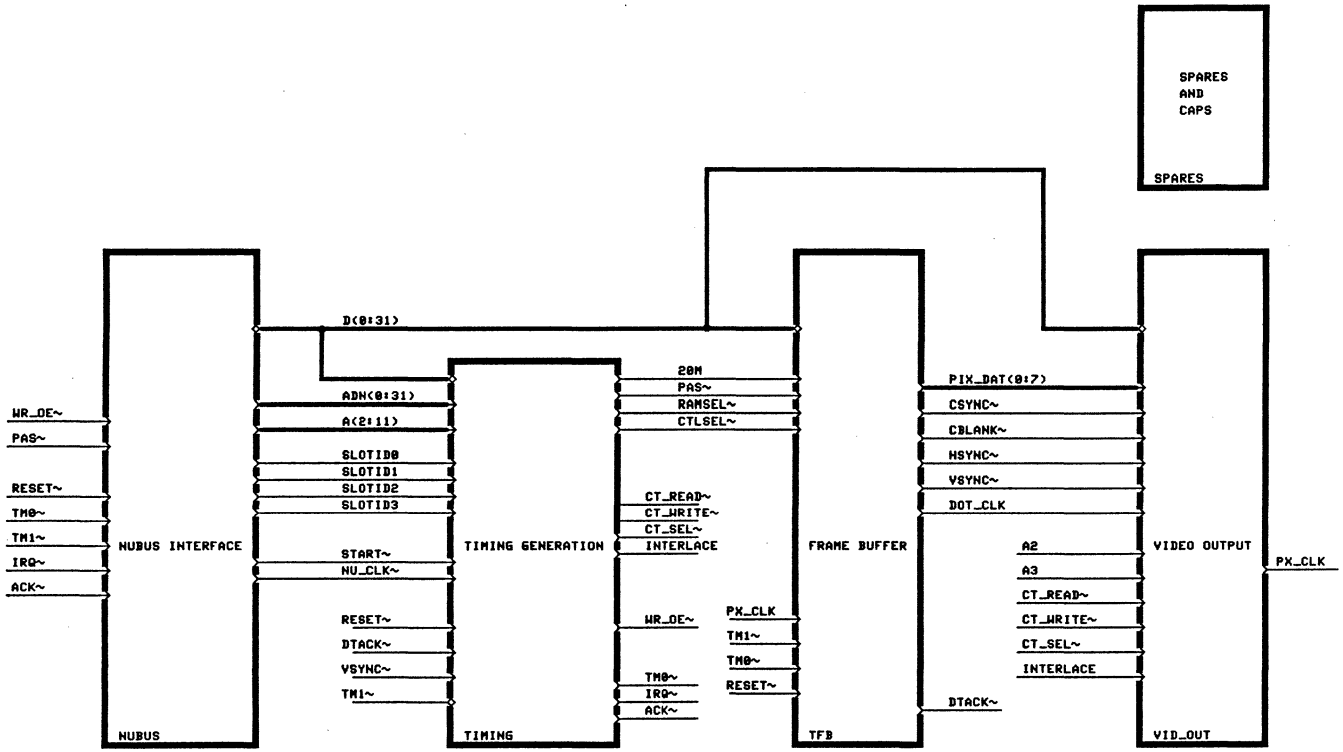

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ORIGINATING DIVISION: ADG	
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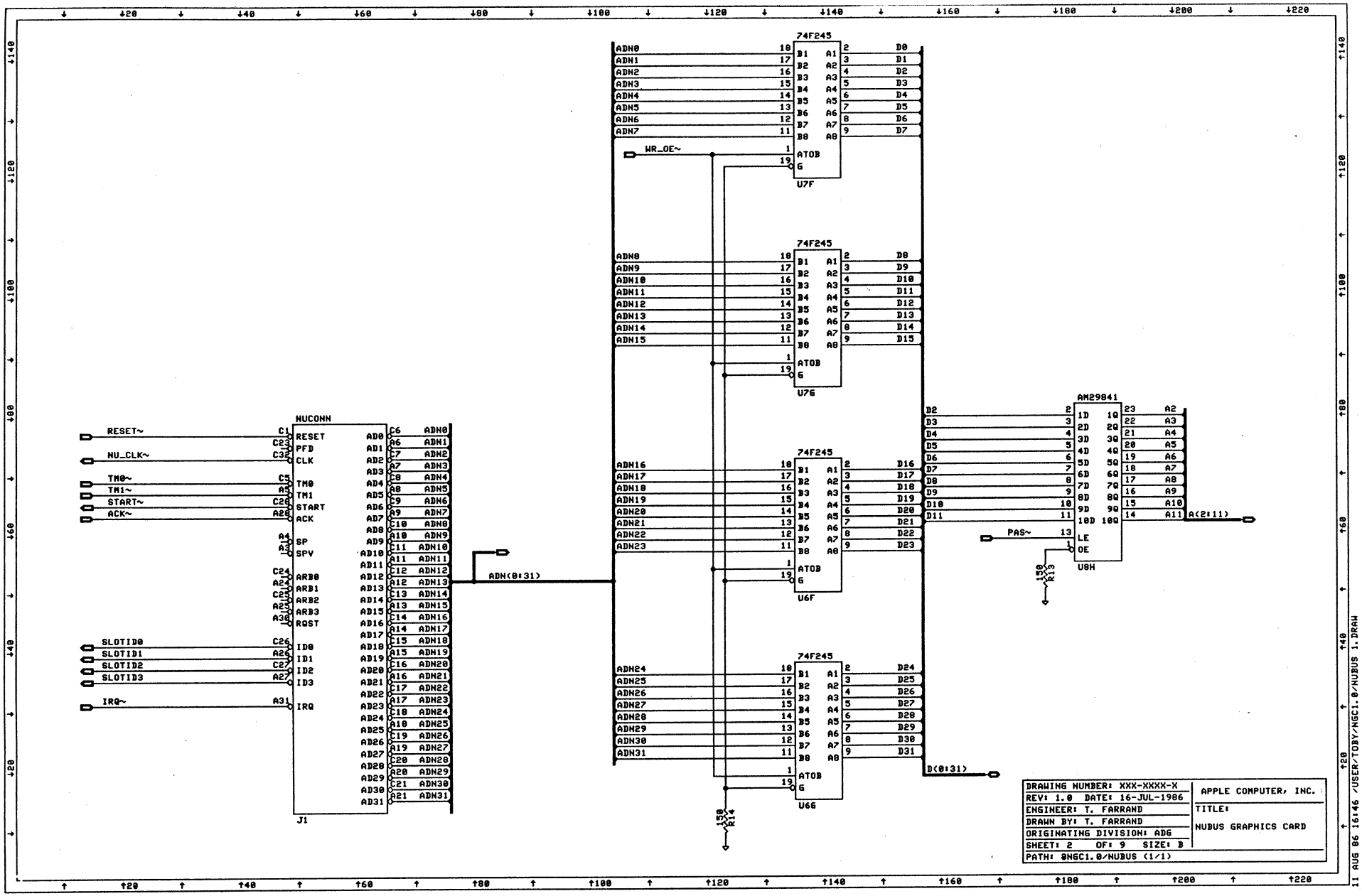
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TM0~
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SLOTID2
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PFD
CLK
TM0
TM1
START
ACK
SP
SPV
ARB0
ARB1
ARB2
ARB3
RQST
ID0
ID1
ID2
ID3
IRQ
AD0
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AD3
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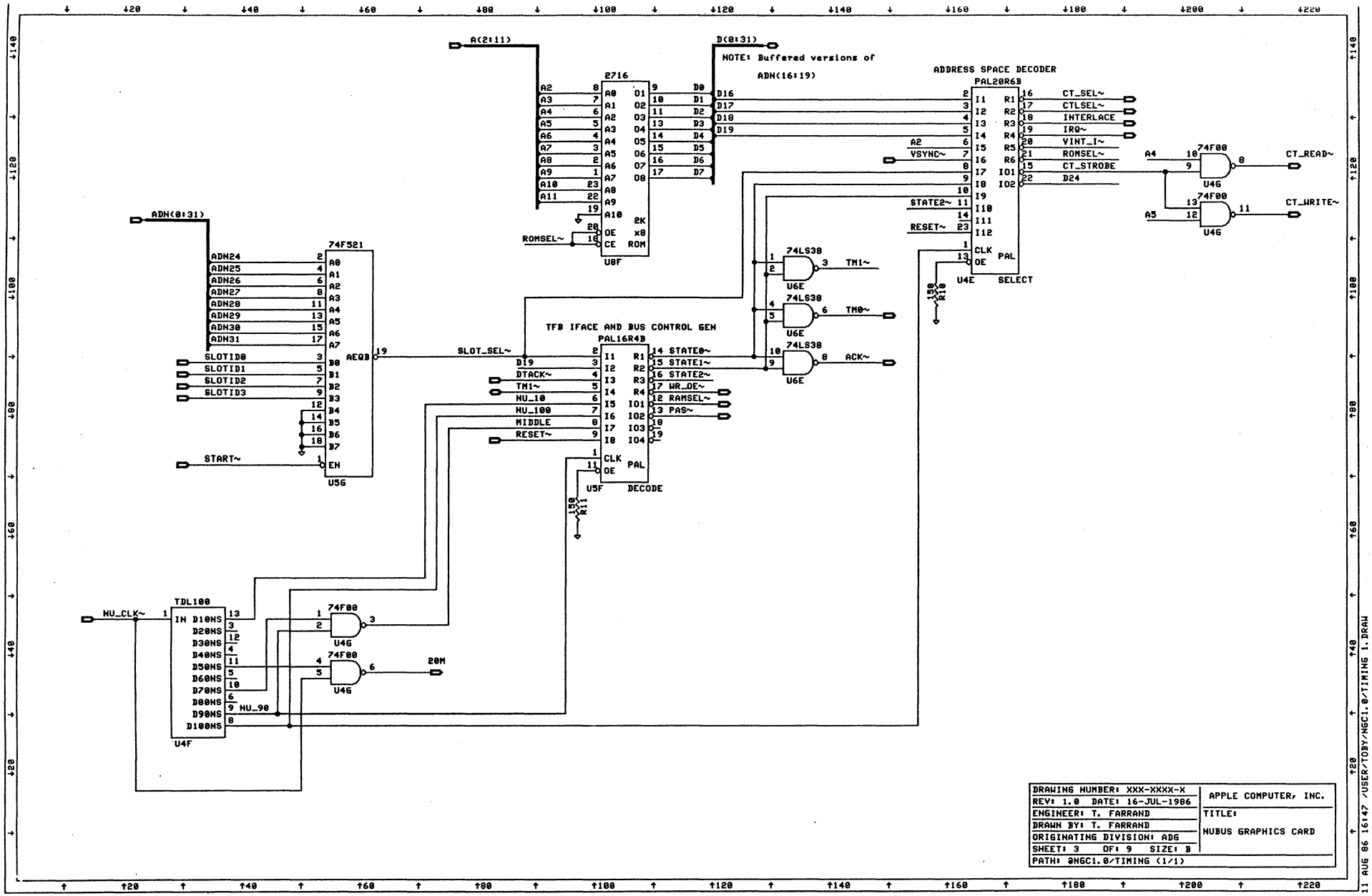

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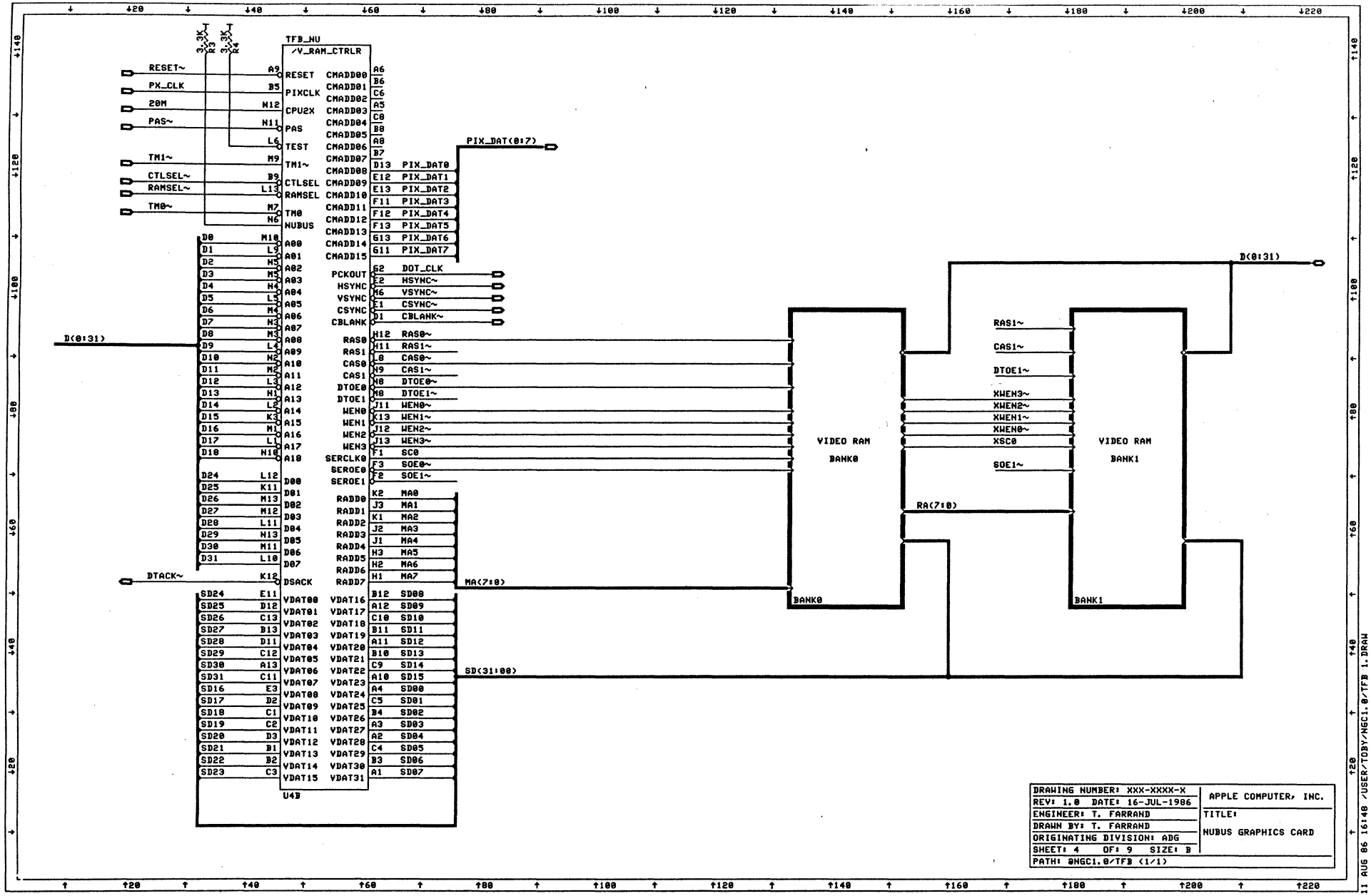
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3.3K R4
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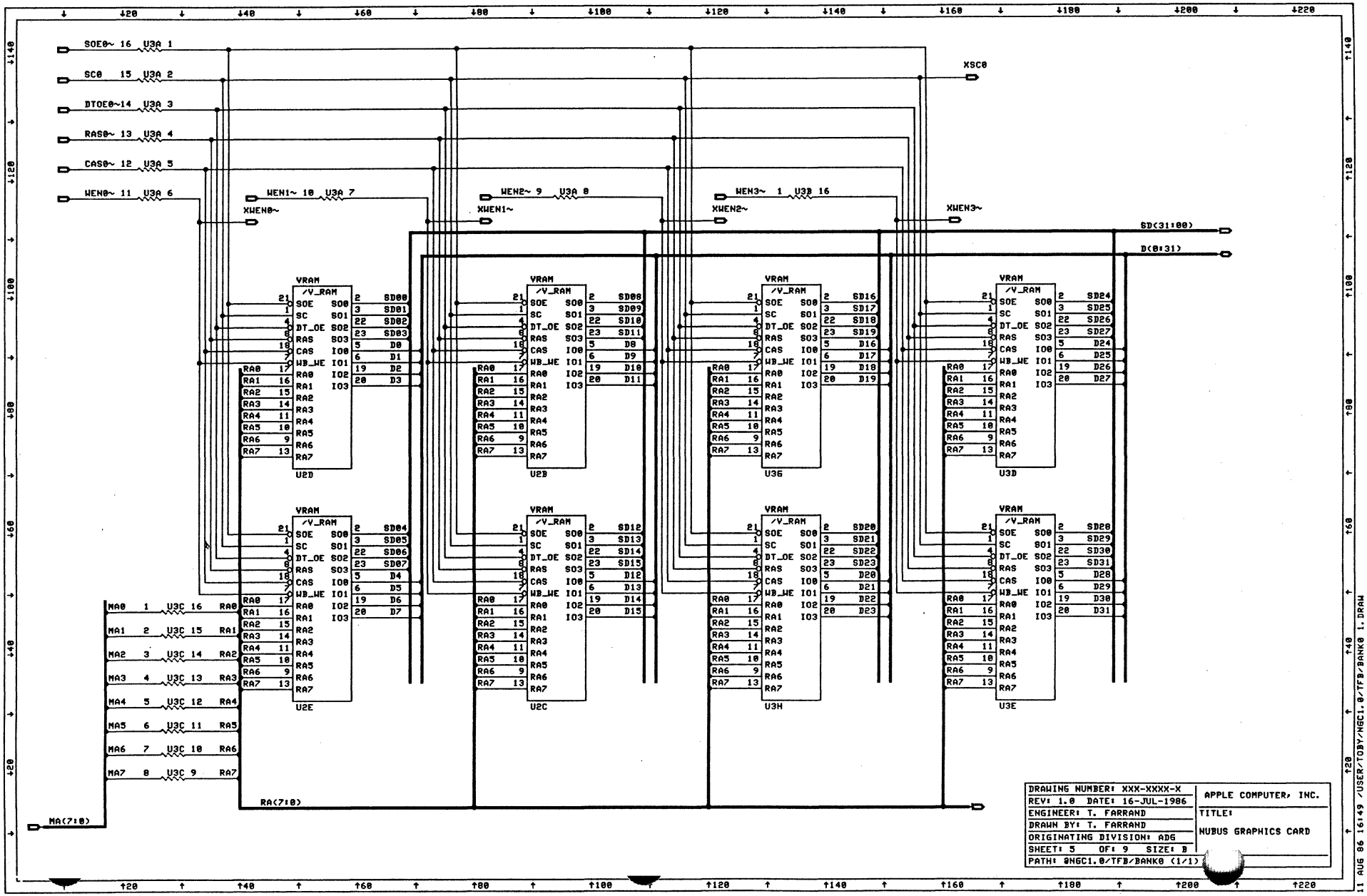
L6
TM1~ M9
CTLSEL~ B9
RAMSEL~ L13
TM0~ M7
N6
DTACK~ K12
D(0:31)
PIX_DAT(0:7)
PIX_DAT0 D13
PIX_DAT1 E12
PIX_DAT2 E13
PIX_DAT3 F11
PIX_DAT4 F12
PIX_DAT5 F13
PIX_DAT6 G13
PIX_DAT7 G11
DOT_CLK G2
HSYNC~ E2
VSYNC~ M6
CSYNC~ E1
CBLANK~ D1
RAS0~ H12
RAS1~ H11
CAS0~ L8
CAS1~ N9
DTOE0~ N8
DTOE1~ M8
WEN0~ J11
WEN1~ K13
WEN2~ J12
WEN3~ J13
SC0 F1
SOE0~ F3
SOE1~ F2
MA0 K2
MA1 J3
MA2 K1
MA3 J2
MA4 J1
MA5 H3
MA6 H2
MA7 H1
MA(7:0)
SD(31:00)
VIDEO RAM BANK0
VIDEO RAM BANK1
RAS1~
CAS1~
DTOE1~
XWEN3~
XWEN2~
XWEN1~
XWEN0~
XSC0
SOE1~
RA(7:0)
BANK0
BANK1
D(0:31)
DRAWING NUMBER: XXX-XXXX-X
REV: 1.0 DATE: 16-JUL-1986
ENGINEER: T. FARRAND
DRAWN BY: T. FARRAND
ORIGINATING DIVISION: ADG
SHEET: 4 OF: 9 SIZE: B
PATH: @NGC1.0/TFB (1/1)
APPLE COMPUTER, INC.
TITLE:
NUBUS GRAPHICS CARD
11 AUG 86 16:48 /USER/TOBY/NGC1.0/TFB 1.DRAW


SOE0~ 16 U3A 1
SC0 15 U3A 2
DTOE0~14 U3A 3
RAS0~ 13 U3A 4
CAS0~ 12 U3A 5
WEN0~ 11 U3A 6
WEN1~ 10 U3A 7
WEN2~ 9 U3A 8
WEN3~ 1 U3B 16
XSC0
XWEN0~
XWEN1~
XWEN2~
XWEN3~
SD(31:00)
D(0:31)
VRAM
/V_RAM
SOE SO0
SC SO1
DT_OE SO2
RAS SO3
CAS IO0
WB_WE IO1
RA0 IO2
RA1 IO3
U2D
U2B
U3G
U3D
U2E
U2C
U3H
U3E
MA0 1 U3C 16 RA0
MA1 2 U3C 15 RA1
MA2 3 U3C 14 RA2
MA3 4 U3C 13 RA3
MA4 5 U3C 12 RA4
MA5 6 U3C 11 RA5
MA6 7 U3C 10 RA6
MA7 8 U3C 9 RA7
MA(7:0)
RA(7:0)
DRAWING NUMBER: XXX-XXXX-X
REV: 1.0 DATE: 16-JUL-1986
ENGINEER: T. FARRAND
DRAWN BY: T. FARRAND
ORIGINATING DIVISION: ADG
SHEET: 5 OF: 9 SIZE: B
PATH: @NGC1.0/TFB/BANK0 (1/1)
APPLE COMPUTER, INC.
TITLE:
NUBUS GRAPHICS CARD
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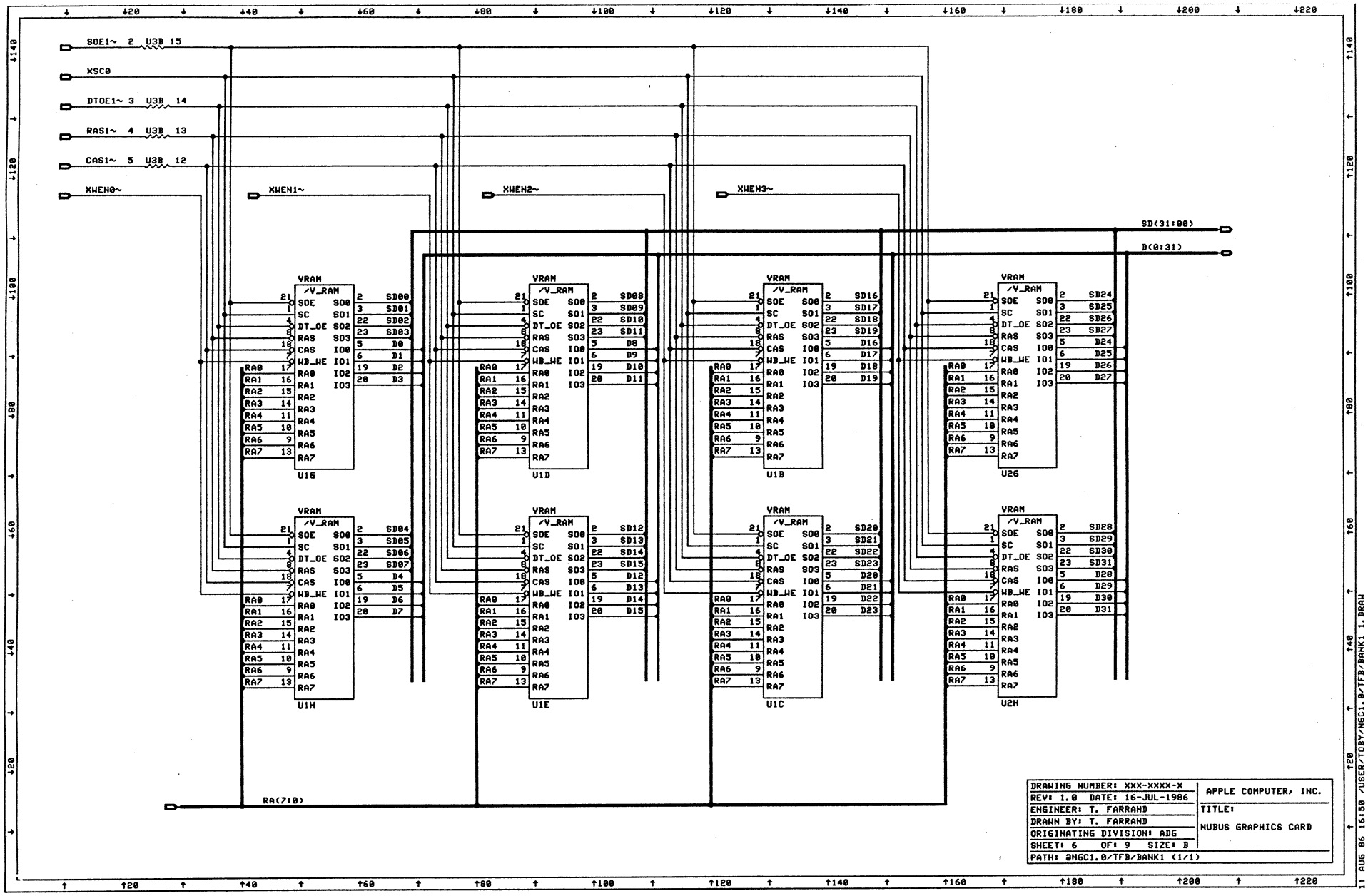
SOE1~ 2 U3B 15
XSC0
DTOE1~ 3 U3B 14
RAS1~ 4 U3B 13
CAS1~ 5 U3B 12
XWEN0~
XWEN1~
XWEN2~
XWEN3~
SD(31:00)
D(0:31)
RA(7:0)
VRAM
/V_RAM
U16
U1D
U1B
U26
U1H
U1E
U1C
U2H
DRAWING NUMBER: XXX-XXXX-X
REV: 1.0 DATE: 16-JUL-1986
ENGINEER: T. FARRAND
DRAWN BY: T. FARRAND
ORIGINATING DIVISION: ADG
SHEET: 6 OF: 9 SIZE: B
PATH: @NGC1.0/TFB/BANK1 (1/1)
APPLE COMPUTER, INC.
TITLE:
NUBUS GRAPHICS CARD
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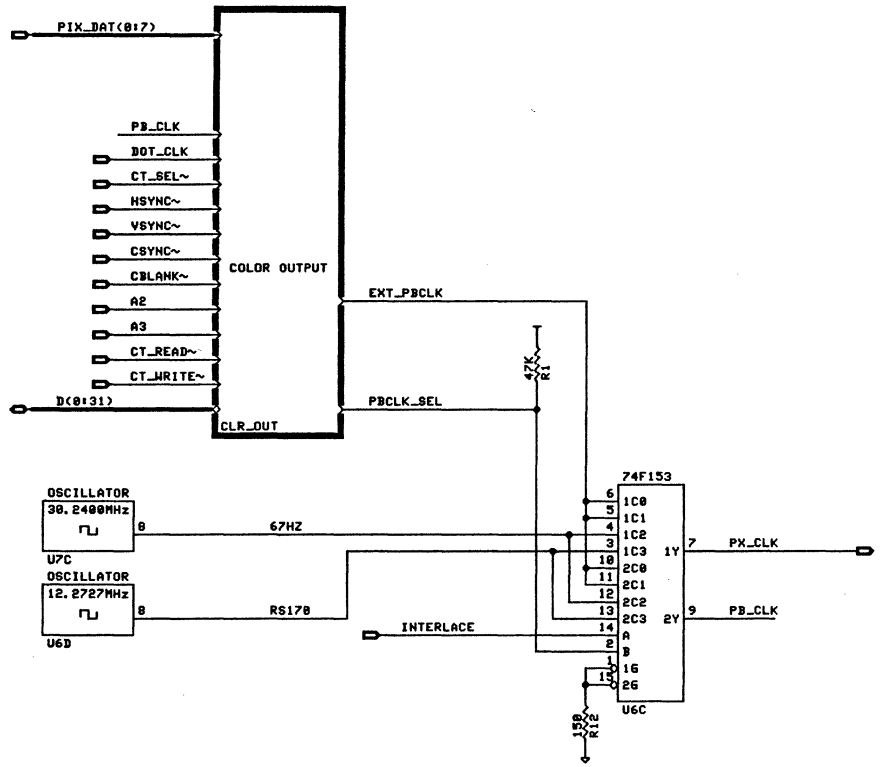

DRAWING NUMBER: XXX-XXXX-X	APPLE COMPUTER, INC.
REV: 1.0 DATE: 16-JUL-1986	
ENGINEER: T. FARRAND	TITLE:
DRAWN BY: T. FARRAND	NUBUS GRAPHICS CARD
ORIGINATING DIVISION: ADG	
SHEET: 7 OF: 9 SIZE: B	
PATH: @NGC1.0/VID_OUT (1/1)	

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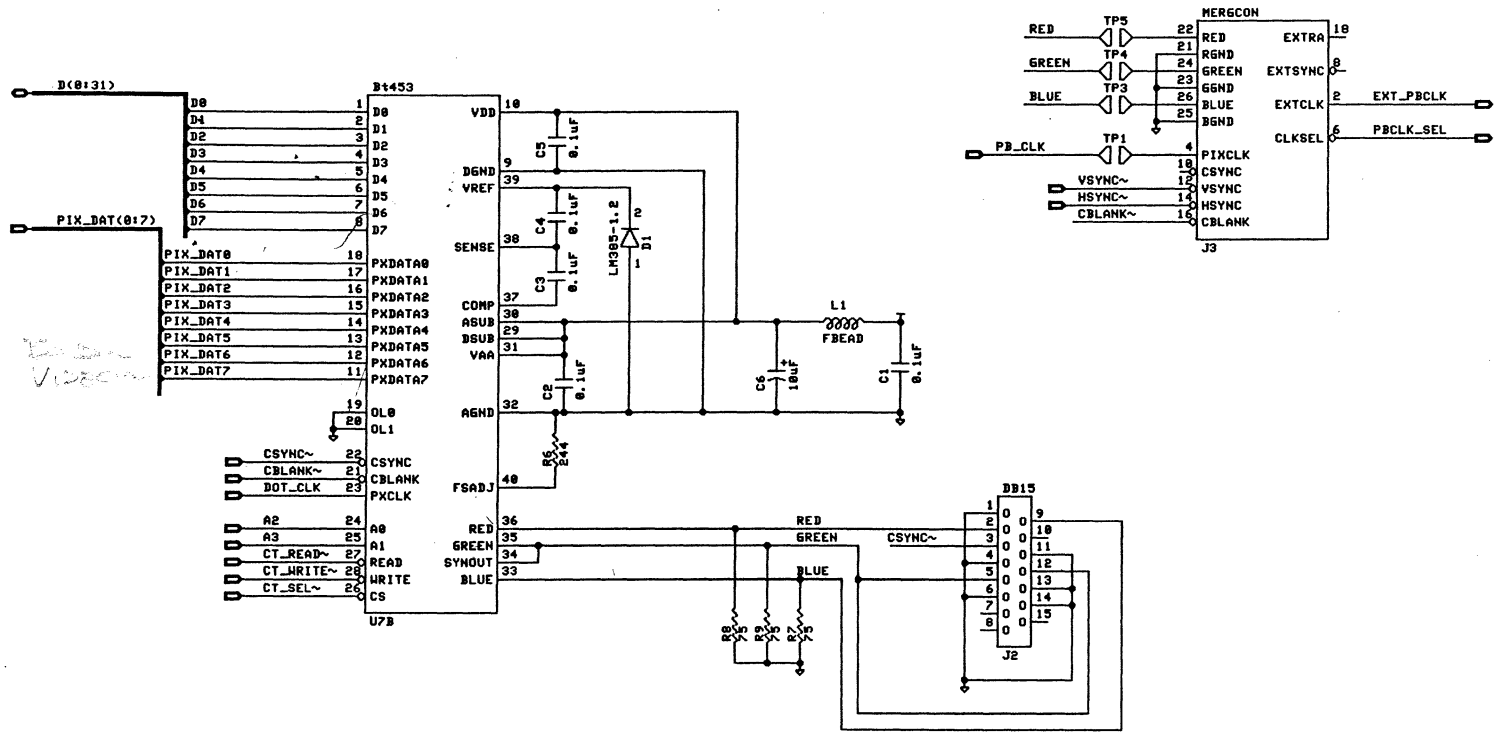
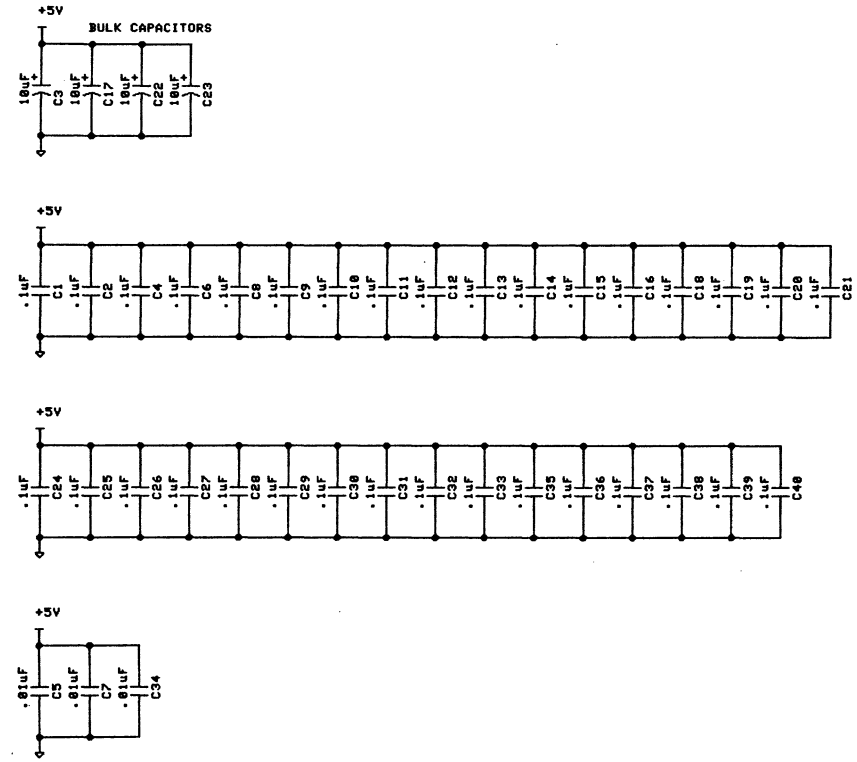


DRAWING NUMBER: XXX-XXXX-X	APPLE COMPUTER, INC.
REV: 1.0 DATE: 16-JUL-1986	
ENGINEER: T. FARRAND	TITLE:
DRAWN BY: T. FARRAND	NUBUS GRAPHICS CARD
ORIGINATING DIVISION: ADG	
SHEET: 8 OF: 9 SIZE: B	
PATH: @N6C1.0/VID_OUT/CLR_OUT (1/1)	

11 AUG 86 16:52 /USER/TOBY/N6C1.0/VID_OUT/CLR_OUT 1.DRAW



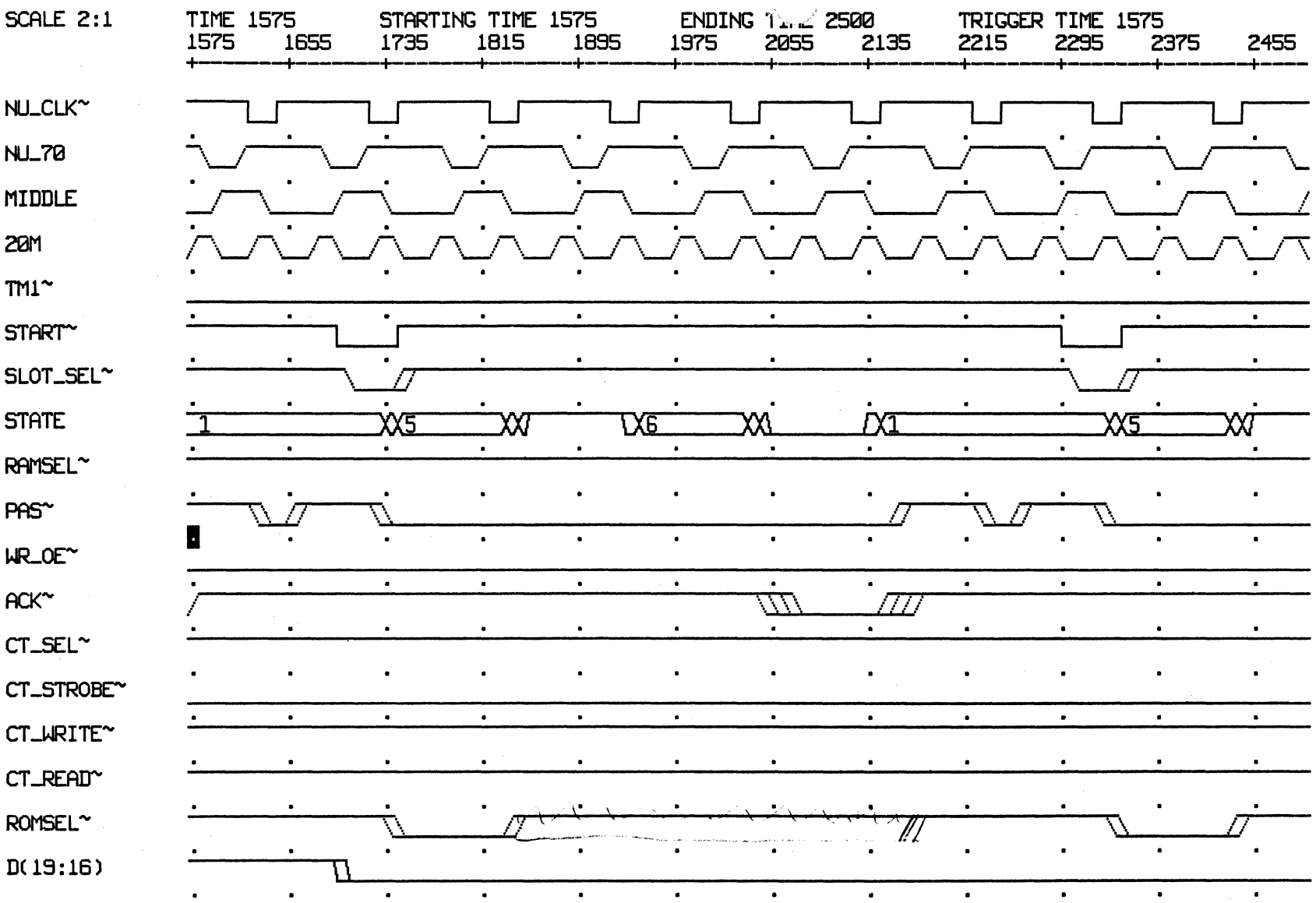
DRAWING NUMBER: XXX-XXXX-X	APPLE COMPUTER, INC.
REV: 1.0 DATE: 16-JUL-1986	
ENGINEER: T. FARRAND	TITLE:
DRAWN BY: T. FARRAND	NUBUS GRAPHICS CARD
ORIGINATING DIVISION: ADG	
SHEET: 9 OF: 9 SIZE: B	
PATH: @NGC1.0/SPARES (1/1)	

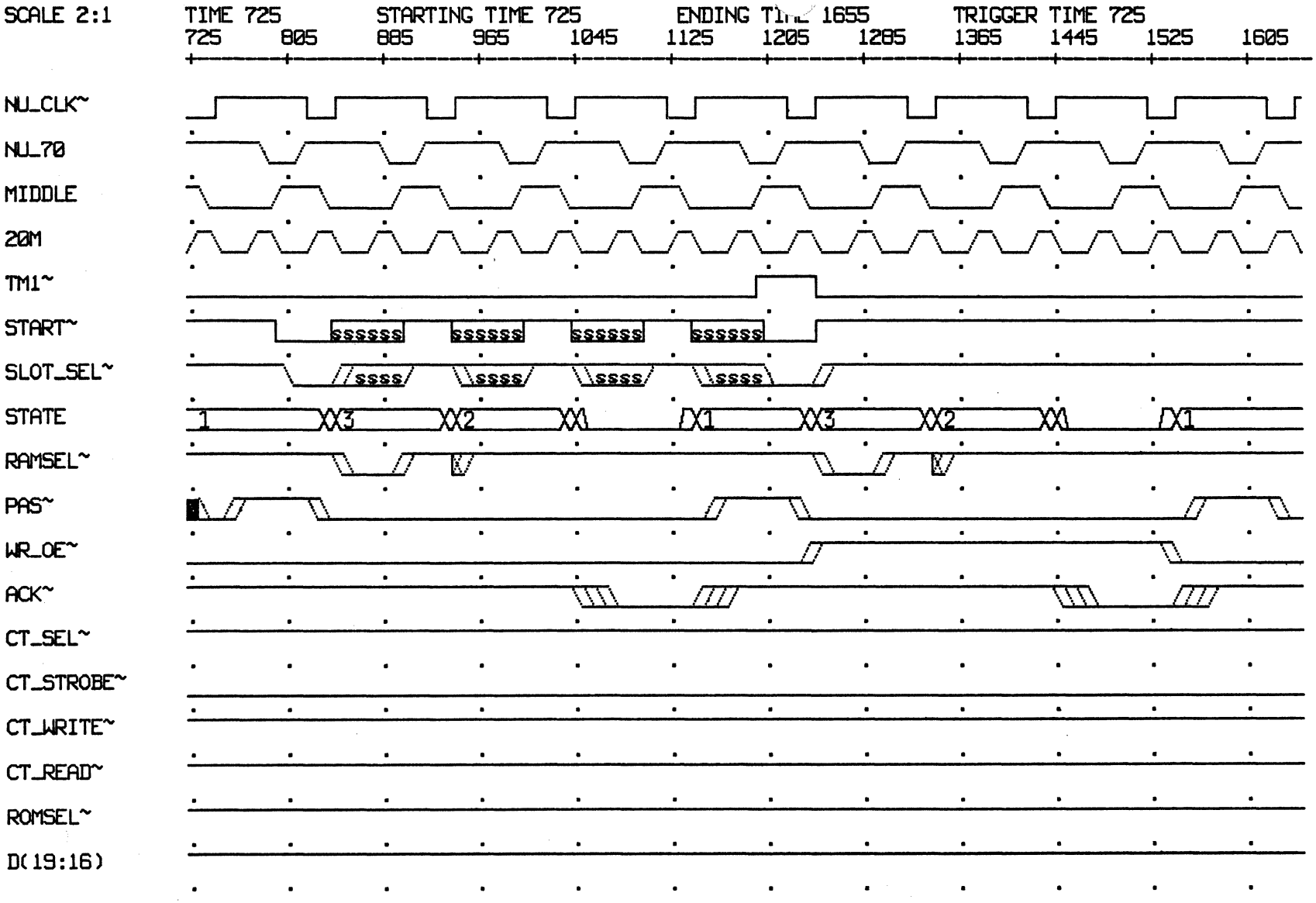
11 AUG 86 16:53 /USER/TOBY/NGC1.0/SPARES 1.DRAW

```
MODULE ngc_decode

TITLE 'NGC decoder - U5F'

"v1.0   1 August 1986 by Toby Farrand

@INCLUDE 'stuff.def'

decode DEVICE 'P16R4';

pindef( clk);           "decoded slot select from NuBus
pindef( slot_sel,N);    "slot_select
pindef( a19,N);         "a19 selects for control spaces or RAM
pindef( dtack,N);       "dtack from TFB
pindef( tm1,N);         "tm1 from NuBus
pindef( nu10);          "no connect input 1
pindef( nu100);         "no connect input 2
pindef( middle,N);      "ok time to change pas signal (ramsel not firing)
pindef( reset,N);       "system reset
pindef( gnd);           "we all know what ground is

pindef( oe,N);
pindef( ramsel,N);      "main ram select
pindef( pas,N);         "pas to the TFB
pindef( state0,N);      "fsm bit 0
pindef( state1,N);      "fsm bit 1
pindef( state2,N);      "fsm bit 2
pindef( read);          "read signal to indicate buffer direction
pindef( nc3);           "no connect output 1
pindef( nc4);           "no connect output 2
pindef( vcc);

fsm = [state2,state1,state0];

EQUATIONS

state0    :=  !state1 #
              (fsm==3) & !dtack #
              reset;

state1    :=  (fsm==1) & slot_sel & !a19 & !reset #
              state1 & state0 & !reset #
              state2 & !state1 & !reset;

state2    :=  (fsm==1) & slot_sel &  a19 & !reset #
              state2 & state0 & !reset;

read      :=  slot_sel & !tm1 #
              read & !(fsm==0) & !reset;

ramsel     =  (fsm==3) & middle;

pas        =  !(nu10 & nu100) # !(fsm==1);

END;
```

```
MODULE ngc_select

TITLE 'NGC select - U4E'

"v1.0   30 July 1986 Toby Farrand

@INCLUDE 'stuff.def'

select DEVICE 'P20R8';

pindef( clk);
pindef( a16,N);
pindef( a17,N);
pindef( a18,N);
pindef( a19,N);
pindef( a2,N);
pindef( vsync,N);
pindef( slot_sel,N);
pindef( state0,N);
pindef( state1,N);
pindef( state2,N);
pindef( gnd);

pindef( oe,N);
pindef( nc1);
pindef( ct_strobe);
pindef( ct_sel,N);
pindef( ctlsel,N);
pindef( interlace,N);
pindef( vint,N);
pindef( vint_i,N);
pindef( romsel,N);
pindef( vsync_i,N);
pindef( reset,N);
pindef( vcc);

EQUATIONS

romsel  := slot_sel &  a19 &  a18 &  a17 &  a16 & !reset #
           romsel &  state2 & !reset #
           romsel &  state1 & !reset #
           romsel &  state0 & !reset;

ct_sel  := slot_sel &  a19 & !a18 & !a17 &  a16 & !reset #
           ct_sel  &  state2 & !reset #
           ct_sel  & !state0 & !reset;

ctlsel  := slot_sel & a19 & !a18 & !a17 & !a16 & !reset #
           ctlsel & state0 & !reset;

"interlace := slot_sel &  a19 & !a18 &  a17 &  a16 #
"             slot_sel & !a19 & interlace #
"             slot_sel &  a18 & interlace #
"             slot_sel & !a17 & interlace #
"             interlace & !slot_sel #
"            reset;

interlace := reset # !reset;

vint    :=  vint & !vint_i & !(slot_sel & a19 & !a18 & a17 & !a16) & !reset #
           !vint & !vint_i & vsync_i & !reset;

vint_i  :=  vint & !vint_i & slot_sel & a19 & !a18 & a17 & !a16 & !reset #
           !vint &  vint_i & vsync_i & !reset;
```

```
ct_strobe := ct_sel & state0 & state2 & !reset;

vsync_i := vsync;

END;
```


SCALE 2:1
TIME 1575
STARTING TIME 1575
ENDING TIME 2500
TRIGGER TIME 1575
1575
1655
1735
1815
1895
1975
2055
2135
2215
2295
2375
2455
NU_CLK~
NU_70
MIDDLE
20M
TM1~
START~
SLOT_SEL~
STATE
1
5
6
1
5
RAMSEL~
PAS~
WR_OE~
ACK~
CT_SEL~
CT_STROBE~
CT_WRITE~
CT_READ~
ROMSEL~
D(19:16)


SCALE 2:1
TIME 725
STARTING TIME 725
ENDING TIME 1655
TRIGGER TIME 725
725
805
885
965
1045
1125
1205
1285
1365
1445
1525
1605
NU_CLK~
NU_70
MIDDLE
20M
TM1~
START~
SLOT_SEL~
STATE
RAMSEL~
PAS~
WR_OE~
ACK~
CT_SEL~
CT_STROBE~
CT_WRITE~
CT_READ~
ROMSEL~
D(19:16)

Preliminary Information

This document contains information on a new product. Characteristic data and other specifications are subject to change without notice.

Bt453

40 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

Distinguishing Features

- 40 MHz Maximum Pipelined Operation
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 3 x 24 Overlay Palette
- RS-343-A Compatible RGB Outputs
- TTL Compatible Interface
- Interfaces easily to any MPU
- +5V CMOS Monolithic Construction
- 40-pin DIP Package
- Power Dissipation: 750 mW Typical

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Personal Computers

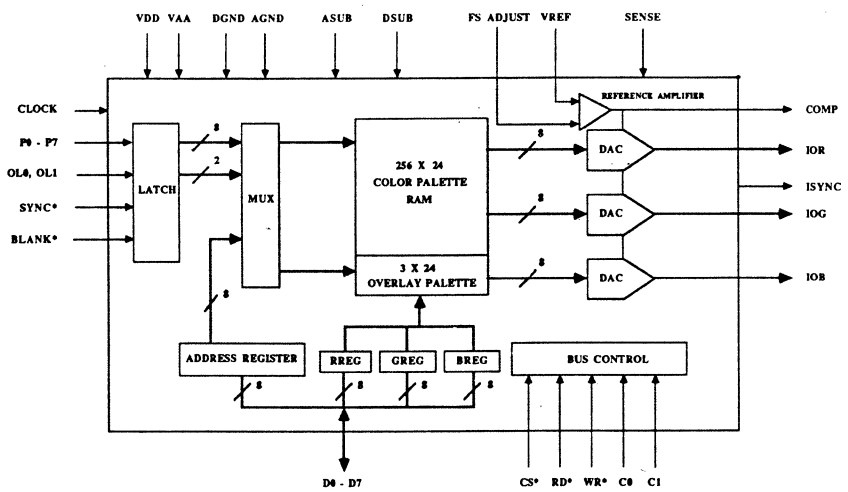
Product Description

The Bt453 is a triple 8-bit video RAMDAC, designed specifically for high resolution color graphics, supporting up to 259 simultaneous colors from a 16.8 million color palette. Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt453 generates RS-343-A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. Differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± 1 LSB over the full temperature range of 0° to +70° C.

Implemented in CMOS for low power dissipation, the Bt453 operates at frequencies up to 40 MHz, and is available in a 40-pin DIP package.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580
TLX 383 596

Brooktree™

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt453 has an internal 256 x 24 color palette RAM and three 24-bit overlay registers, allowing the display of up to 259 simultaneous colors from a 16.8 million color palette. The MPU bus interface operates asynchronously to the video data, simplifying the design interface.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM, or the overlay registers, as shown in table 1. The upper eight bits of the address register increment following reading or writing blue color information, and are used to specify which palette entry is being accessed, as illustrated in table 2. The two least significant bits count modulo 3, specifying red, green, and blue data, and are reset to zero anytime the MPU writes to the address register.

When writing to the palettes, the red and green values are temporarily stored in registers, and during the blue value write cycle, all 24 bits of color information are written to the palettes. While the MPU is writing blue data or reading red, green, or blue data, the Bt453 forces any pixels addressed by the P0 - P7, OL0, and OL1 inputs to the reference black level. To avoid contention between MPU accesses to the palettes and video refresh, the palettes should only be accessed during retrace intervals.

Table 3 illustrates the truth table for MPU accesses, and figure 1 illustrates the MPU read/write timing.

Video Generation

As illustrated in figure 2, on the rising edge of each CLOCK cycle, eight bits of color information (P0 - P7) and two bits of overlay information (OL0, OL1) are latched into the device. This data is used to specify which palette entry is to be used to provide color information. The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character, cursor, or grid generation logic. Table 4 illustrates the truth table used for color selection.

On every CLOCK cycle, the selected 24 bits of color information (8 bits each of red, green, and blue) are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, also sampled on the rising edge of each CLOCK cycle and pipelined to maintain synchronization with the pixel and overlay data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in figure 3. The varying current from each of the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Note that the Bt453 has a separate current output for the composite sync information (ISYNC). By externally connecting ISYNC to the green output (IOG), sync information may be encoded on the green channel. Table 5 details how SYNC* and BLANK* modify the output levels.

The D/A converters on the Bt453 use a segmented architecture, eliminating the need for precision component ratios and greatly reducing the switching transients. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs.

CRT Monitor Interface

As illustrated in figure 4, the analog outputs (IOR, IOG, IOB) each drive a 37.5 ohm (typical) load, such as a doubly-terminated 75-ohm coaxial load.

C1	C0	Function addressed by MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

Table 1. Control Input Truth Table.

Circuit Description (continued)

		Value	C1	Addresses
ADDR0 - 1	counts modulo 3,	00 01 10		red value green value blue value
ADDR2 - 9	counts binary,	$00 - $FF $00 $01 $02 $03	0 1 1 1 1	color palette RAM reserved overlay color 0 overlay color 1 overlay color 2

Table 2. Address Register (ADDR) Operation.

RD*	WR*	C0	ADDR1	ADDR0	Function
1	0	0	x	x	write address register; D0 - D7 --> ADDR2 - 9, 0 --> ADDR0 - 1
1	0	1	0	0	write red value; increment ADDR0 - 9
1	0	1	0	1	write green value; increment ADDR0 - 9
1	0	1	1	0	write blue value; update entry, increment ADDR0 - 9
0	1	0	x	x	read address register; ADDR2 - 9 --> D0 - D7
0	1	1	0	0	read red value; increment ADDR0 - 9
0	1	1	0	1	read green value; increment ADDR0 - 9
0	1	1	1	0	read blue value; increment ADDR0 - 9
0	0	x	x	x	illegal operation

Table 3. Truth Table for MPU Read/Write Operations (CS = 0).*

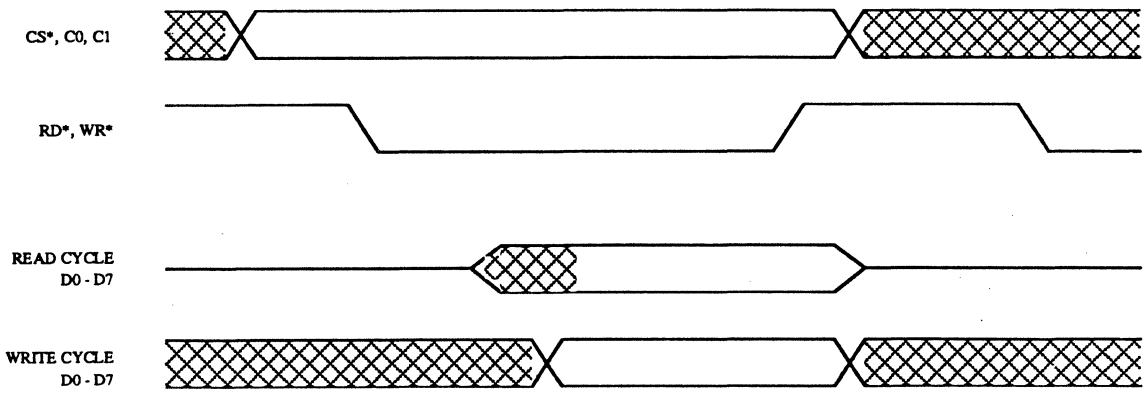


Figure 1. Host MPU Read/Write Timing.

OL1	OL0	P7 - P0	Addresses
0	0	$00	color palette entry $00
0	0	$01	color palette entry $01
.	.	.	.
.	.	.	.
0	0	$FF	color palette entry $FF
0	1	$xx	overlay color 0
1	0	$xx	overlay color 1
1	1	$xx	overlay color 2

Table 4. Pixel Select and Overlay Control Truth Table.

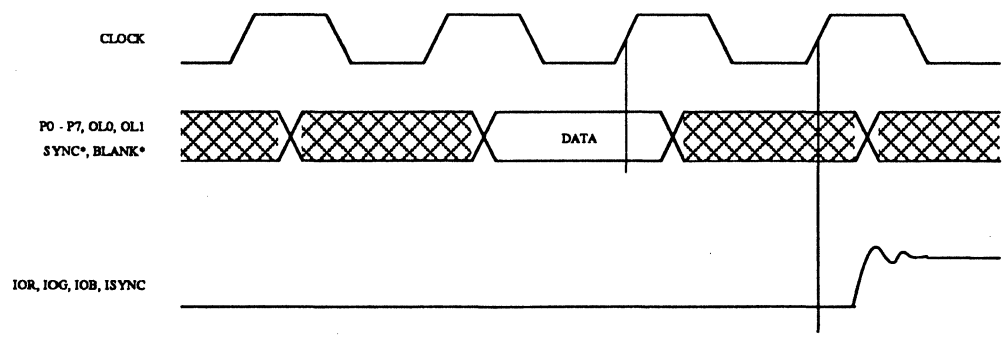
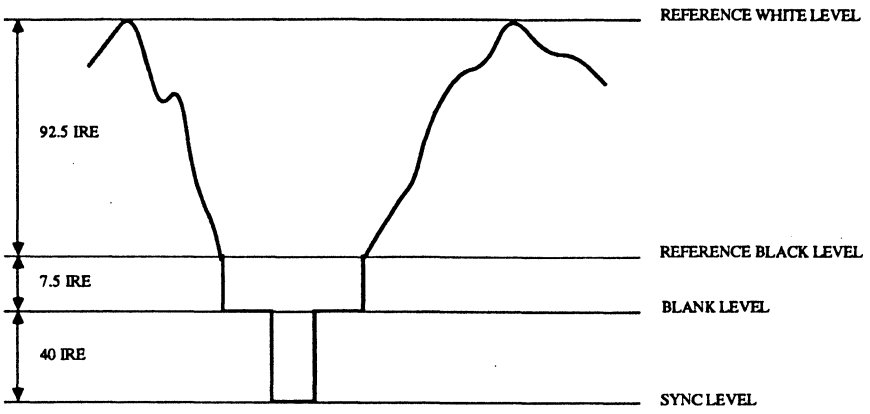


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.34
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-ohm doubly-terminated load, VREF = 1.2 volts, RSET = 274 ohms, ISYNC output connected directly to the IOG output. RS-343-A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR (mA)	IOB (mA)	SYNC*	BLANK*	DAC Input Data
REF WHITE	26.67	19.05	19.05	1	1	$FF
REF BLACK	9.05	1.44	1.44	1	1	$00
BLANK	7.62	0.00	0.00	1	0	$xx
DATA - SYNC	data - 7.62	data	data	0	1	data
SYNC	0.00	0.00	0.00	0	0	$xx

Note: Typical with full scale IOG = 26.67 mA, IOR = 19.05 mA, and IOB = 19.05 mA. RSET = 274 ohms, VREF = 1.2 volts, ISYNC output connected directly to IOG output.

Table 5. Video Output Truth Table.

Pin Descriptions

Pin Name	Pin Number	Description
BLANK*	21	Composite blank control input (TTL compatible). A logic zero overrides the P0 - P7, OL0, and OL1 inputs and forces the IOR, IOG, and IOB outputs to the blanking level, as illustrated in table 4. It is continuously sampled on the rising edge of CLOCK.
SYNC*	22	Composite sync control input (TTL compatible). A logical zero on this input switches off the ISYNC current output. SYNC* does not override any other command or data input, as shown in table 4; therefore, it should be asserted only during the blanking interval. It is continuously sampled on the rising edge of CLOCK.
P0 - P7	18, 17, 16, 15, 14, 13, 12, 11	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are continuously sampled on the rising edge of CLOCK.
OL1, OL0	19, 20	Overlay select inputs (TTL compatible). These control inputs are continuously sampled on the rising edge of CLOCK and specify which palette is to be used for color information, as follows:

OL1	OL0	
0	0	color palette RAM
0	1	overlay color 0
1	0	overlay color 1
1	1	overlay color 2

When accessing the overlay palette, the P0 - P7 inputs are ignored. Overlay information bits (up to two bits per pixel) are input through this port.

IOR	36	Red video output. This high impedance current source directly drives a doubly-terminated 75-ohm coaxial cable (figure 4).
IOG	35	Green video output. This high impedance current source directly drives a doubly-terminated 75-ohm coaxial cable (figure 4).
IOB	33	Blue video output. This high impedance current source directly drives a doubly-terminated 75-ohm coaxial cable (figure 4).
ISYNC	34	Sync current output. Typically, this current output is directly wired to the IOG output, and enables sync information to be encoded on the IOG output. A logical one on the SYNC* input results in 7.62 mA (typical) being output onto this pin, and a logical zero results in no current being output on this pin.
CLOCK	23	Clock input (TTL compatible). P0 - P7, OL0, OL1, SYNC*, and BLANK* are all latched with respect to the rising edge of CLOCK. It is typically the pixel clock rate of the video system.

Pin Descriptions (continued)

Pin Name	Pin Number	Description
AGND	32	Analog ground. This pin should be used as the return point for the output termination resistors by externally connecting it to the IOR, IOG, and IOB outputs through 75-ohm resistors (figure 4).
VAA	31	Analog power. The Bt453 uses separate analog and digital power supplies to provide the highest possible noise immunity; however, it is recommended that VAA and VDD be connected to the same power source with individual high-frequency decoupling capacitors (figure 4).
DGND	9	Digital ground.
VDD	10	Digital power. The Bt453 uses separate analog and digital power supplies to provide the highest possible noise immunity; however, it is recommended that VAA and VDD be connected to the same power source with individual high frequency decoupling capacitors (figure 4). VDD must not be greater than VAA + 0.3 volts, even under power-up conditions. See recommended operating conditions.
ASUB, DSUB	30, 29	Analog and digital substrate pins. These pins should be connected directly to VAA, as illustrated in figure 4.
COMP	37	Compensation output pin. This signal provides compensation for the internal reference amplifier. A 0.1 µF capacitor must be connected between this pin and SENSE (figure 4).
SENSE	38	Sense pin. A 0.1 µF capacitor must be connected between this pin and COMP (figure 4).
FS ADJUST	40	Full scale adjust control input. A resistor (RSET) connected between this input and AGND controls the magnitude of the full scale video signal. See figure 4.
VREF	39	Voltage reference input. This input must be held between +1.14 volts and +1.26 volts by using an external temperature-compensated reference circuit such as the one shown in figure 4. An external 0.1 µF capacitor must also be connected between this pin and SENSE.
CS*	26	Chip select control input (TTL compatible). This input must be a logical zero to enable the MPU to write data to or read data from the device. See figure 1.
RD*	27	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See figure 1.
WR*	28	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. MPU write data is latched on the rising edge of WR*. See figure 1.
C0, C1	24, 25	Command control inputs (TTL compatible). C0 and C1 specify which internal control register or color palette the MPU is accessing, as illustrated in table 1.
D0 - D7	1, 2, 3, 4, 5, 6, 7, 8	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bi-directional data bus.

PC Board Layout Considerations

PC Board Considerations

It is recommended that a four layer PC board, with power and ground planes inside the board and signals on the top and bottom of the board, be used.

Further information on PC board layout practices for high-speed D/A converters may be found in Brooktree Application Note AN-1.

Ground Planes

Best performance is obtained by separating the ground plane of the PC board into two separate areas, designated as digital ground and analog ground, with at least an 1/8" gap between the areas. The digital ground plane should encompass the area under all the digital logic, including the digital signal traces leading up to the RAMDAC, but excluding any ground pins on the RAMDAC. The analog ground plane area should include all RAMDAC ground pins (AGND and DGND), all reference and power supply bypass circuitry for the RAMDAC, the analog output traces, and the video output connectors. The digital and analog ground planes should be connected at a single point by a ferrite bead, as illustrated in figure 4. This bead should be located within an inch of the RAMDAC.

Power Planes

The power plane of the PC board should also be separated into two areas, designated as digital power and analog power, which lay on top of the digital and analog ground planes. The digital plane will supply power to all digital logic on the PC board and the analog power plane will supply all power pins of the RAMDAC (VAA, VDD, ASUB, and DSUB), together with power for the reference circuitry. It is important that portions of the digital power plane do not overlay portions of the analog ground plane and that portions of the analog power plane do not overlay portions of the digital ground plane. This will reduce plane-to-plane noise coupling. The digital and analog power planes should be connected together at a single point by a ferrite bead, as illustrated in figure 4. This bead should be located within an inch of the RAMDAC.

Power and ground connections from the PC board to the power supply should be made to the digital power and ground planes.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best RAMDAC performance, a 0.1 μF ceramic capacitor in parallel with a 0.01 μF chip capacitor should be placed as close as possible to each RAMDAC power pin, for bypassing the analog power and ground planes. If chip capacitors are not feasible, radial lead ceramic capacitors may be used.

It is important to note that while the RAMDAC contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the RAMDAC should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power plane areas of the PC board.

Due to the high clock rates involved, long clock lines to the RAMDAC should be avoided to reduce noise pickup.

Analog Signal Interconnect

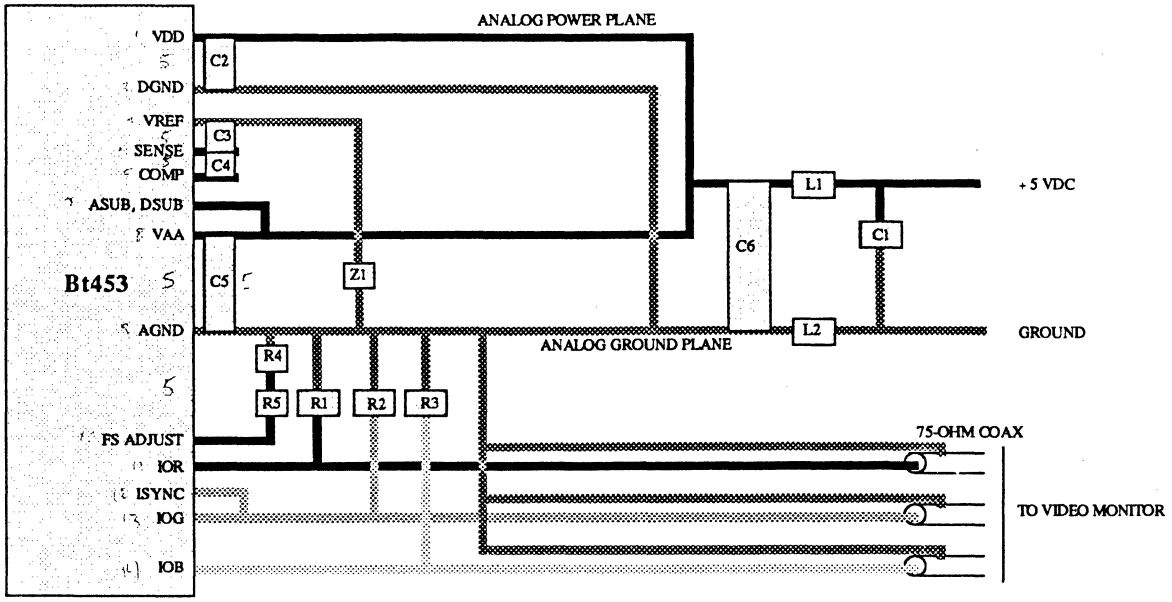
The RAMDAC should be located as close as possible to the video output connectors to minimize noise pickup, and reflections due to impedance mismatch. Also, the external analog reference circuitry should be as close as possible to the RAMDAC to avoid noise pickup.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Output Load (RL)

For maximum performance, each of the three current outputs should have a 75-ohm load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the RAMDAC to minimize reflections.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2, C3, C4, C5	0.1 µF ceramic capacitor	Mallory CK05BX104K
C6	10 µF tantalum capacitor	Mallory CSR13-G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-ohm, 1% metal film resistor	Dale CMF-55C, 75 ohms
R4	50 ohm, 1 turn cermet potentiometer	Bourns 3329P-12F9605, 50 ohms
R5	243-ohm, 1% metal film resistor	Dale CMF-55C, 243 ohms
Z1	1.2-volt voltage reference	National Semiconductor LM385BZ-1.2

Note: The above listed vendor numbers are listed only as a guide. Substitution with devices of similar characteristics will not affect the performance of the RAMDAC.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

Voltage Reference

It is recommended that a temperature compensated voltage reference, such as the one listed in figure 4, be used for providing the 1.2v reference supply (VREF). This ensures reliable and stable operation over the entire recommended temperature range.

The Bt453 has an internal pullup resistor between the VREF input and VAA. As the value of this resistor may vary slightly due to process variations, the use of a resistor divider network to generate the 1.2v reference voltage is not recommended.

FS ADJUST Resistor (RSET)

As shown in figure 4, resistors R4 and R5, combined to form RSET, are used to control the full scale current output of the RAMDAC. RSET has a typical value of 274 ohms, for generation of RS-343-A video when driving a 37.5-ohm load, but may be varied to enable generation of voltage levels other than RS-343-A. Note that the IRE relationships illustrated in figure 3 are maintained, regardless of the full-scale output current. Figure 5 illustrates the typical output current values versus RSET.

A single metal film precision resistor may be used in place of R4 and R5 to reduce component count and eliminate manual adjustments of the output current.

CRT Monitor Interfacing

When ISYNC is externally connected directly to the green output (IOG), the Bt453 generates a zero volt sync tip on the green channel. As most CRT monitors have AC-coupled video inputs, the RAMDAC should be capable of interfacing directly to the CRT monitor.

To generate a -0.286v sync tip for RS-343-A applications, a circuit similar to the one illustrated in figure 5 may be used. Other applications may require a different amount of sync current other than the 7.62 mA (0.00762) used in the example.

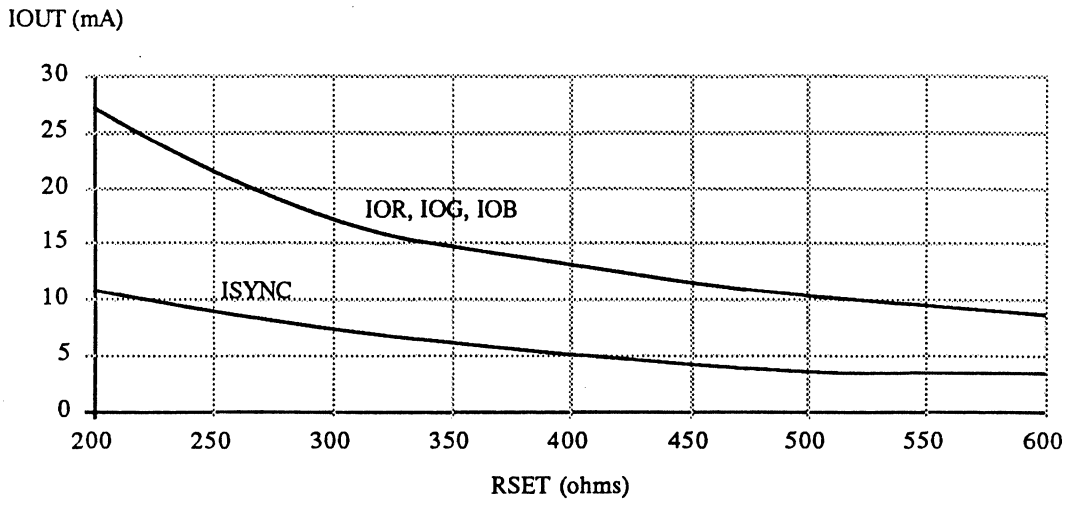
If sync information is not to be encoded on the green channel, ISYNC should not be connected to the IOG output. In this instance, the IOG output will not be level shifted from the IOR and IOB outputs.

If driving an excessive amount of coaxial cable, the designer may wish to buffer the video analog signals prior to driving the coax.

Typical Application

Table 6 illustrates how the Bt453 operates in a variety of graphics environments. Figure 7 illustrates using the Bt453 RAMDAC in a typical color graphics application.

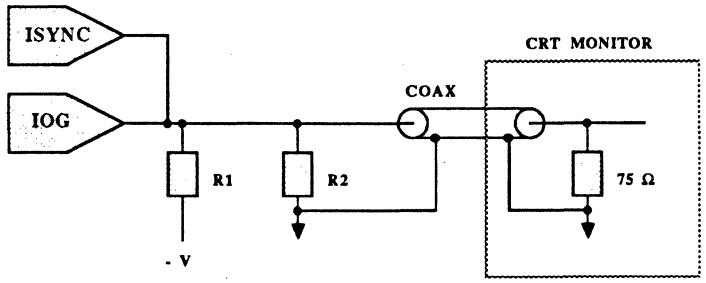
Application Information (continued)



IOR, IOG, IOB = (VREF) (4.3498) / RSET ISYNC = (VREF) (1.7399) / RSET

Note: VREF = 1.2 volts, TA = 25° C. SYNC* and BLANK* are a logical one. Input data to the D/A converters are $FF. ISYNC not connected to IOG.

Figure 5. Maximum IOUT versus RSET.



R1 || R2 = 75 Ω

R1 = (V - 0.286) / 0.00762

Figure 6. Generation of -0.286v Sync Tip.

Application Information (continued)

Resolution (pixels) Video Rate	512 x 512 20 MHz	640 x 400 20 MHz	640 x 480 25 MHz	768 x 576 35 MHz
256K DRAMs / bit plane	1	1	2	2

Table 6. Typical Applications for the Bt453.

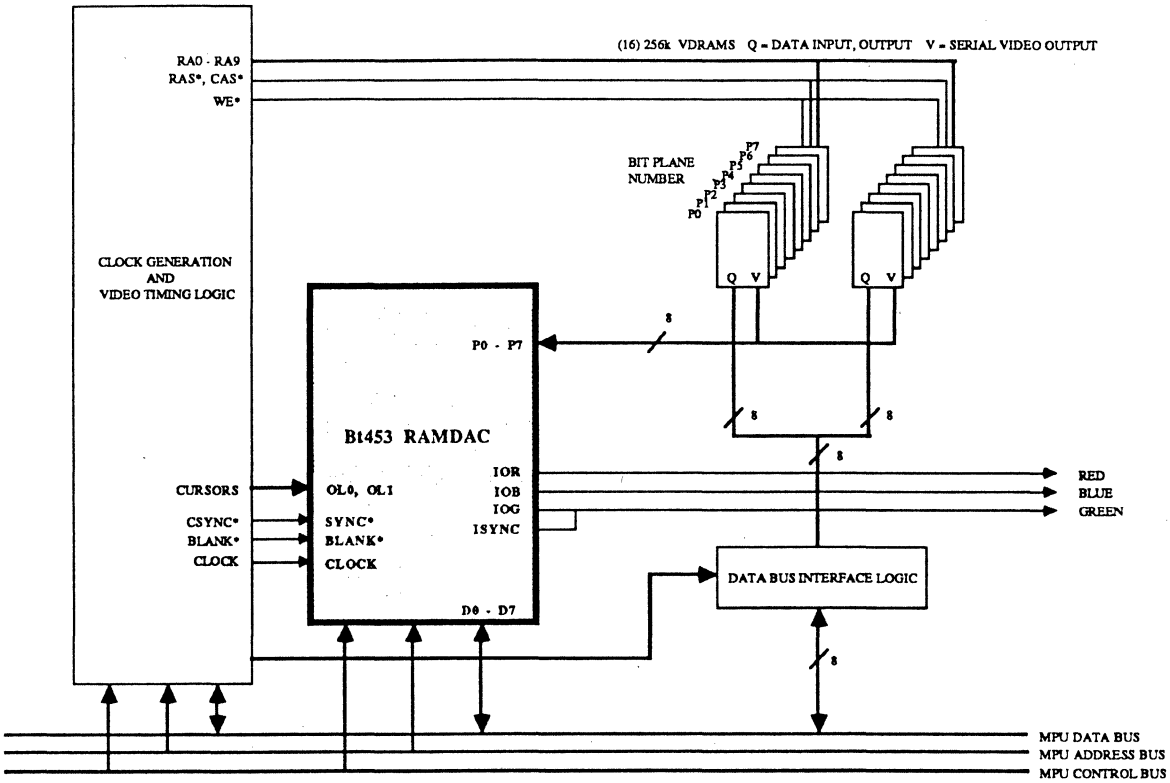


Figure 7. Typical Application of the Bt453.
(640 x 480 pixels, 256 colors from a 16.8 million color palette)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Power	VAA, VDD	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+ 70	°C.
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.2	1.26	Ohms
FS ADJUST Resistor	RSET		274		

Note: VAA and VDD should be attached to a common power supply with appropriate bypass circuitry. If separate supplies are used, VDD should never exceed VAA by more than 0.3 volts under any circumstances, including power-up sequencing.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
VDD (measured to DGND)				VAA + 0.3	Volts
Voltage on any Pin		AGND - 0.3		VAA + 0.3	Volts
Voltage Difference between AGND and DGND				0.5	Volts
Output Short-Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 175	°C.
Soldering Temperature (5 seconds, 1/4 inch from pin)	TSOL			260	°C.
Power Dissipation	PD			1000	mW
Package Derating				5.5	mW / °C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics (Over Recommended Operating Conditions)

Paramcter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity	IL	- 1		+ 1	LSB
Differential Linearity	DL	- 1		+ 1	LSB
Full Scale Error		- 5		+ 5	% of FSR
Zero Error		- 5		+ 5	% of FSR
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VDD + 0.5	Volts
Input Low Voltage	VIL	DGND - 0.5		0.8	Volts
Input High Current (Vin = 2.4v)	IIH			10	µA
Input Low Current (Vin = 0.4v)	IIL			10	µA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN			10	pF
Digital Outputs					
Output High Voltage	VOH	2.4			Volts
Output Low Voltage	VOL			0.4	Volts
Output Low Current (VOL = 0.4v)	IOL	3.2			mA
Output High Current (VOH = 2.4v)	IOH	400			µA
3-State Current	IOZ			10	µA
Output Capacitance	CDO			20	pF
Analog Outputs					
Output Current (Note 1)	IOR, IOG,				
White Level	IOB	18.10	19.05	20.00	mA
Black Level		1.37	1.44	1.51	mA
Blank Level			0.00		mA
Output Current (Note 1)	ISYNC				
Sync Level (SYNC* = 1)		7.24	7.62	8.0	mA
Sync Level (SYNC* = 0)			0.00		mA
DAC to DAC Matching			2		%
Output Compliance (1 LSB IL)	VOC	- 1.0		+ 1.2	Volts
Output Capacitance (f = 1 MHz, IOR, IOG, IOB, ISYNC = 0)	CAO			20	pF
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.3		% / % VAA

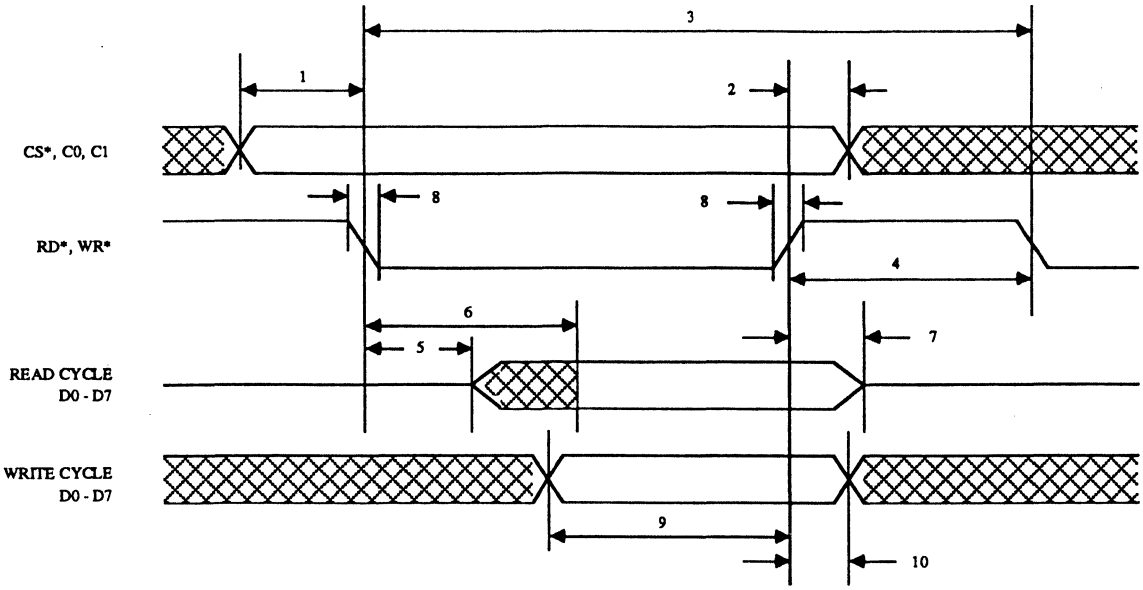
Note 1: Test conditions: RSET = 274 Ω, VREF = 1.235v, RL = 37.5 Ω, ISYNC not connected to IOG.

A. C. Characteristics (Over Recommended Operating Conditions)

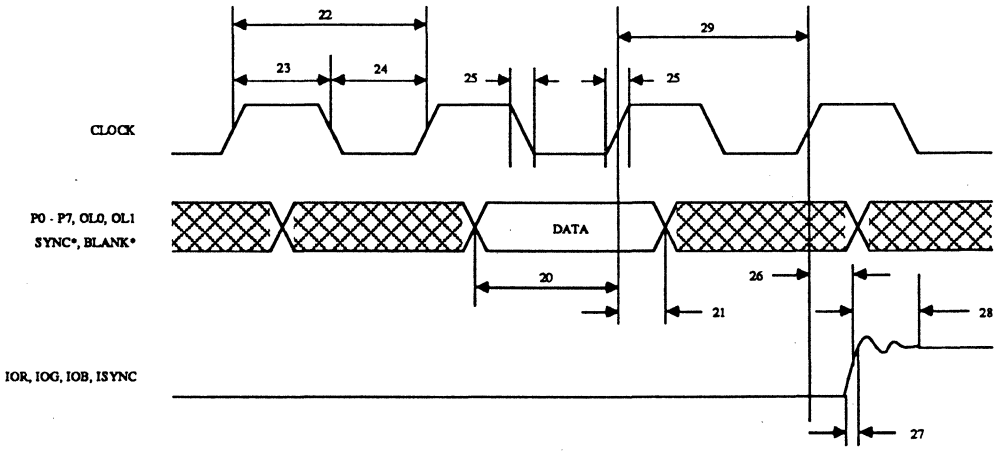
Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			40	MHz
CS*, C0, C1 Setup Time	1	35			ns
CS*, C0, C1 Hold Time	2	35			ns
MPU Cycle Time	3	150			ns
RD*, WR* High Time	4	25			ns
RD* Asserted to Data Bus Driven (Data Bus CL = 50 pF)	5	10			ns
RD* Asserted to Data Valid (Data Bus CL = 50 pF)	6			100	ns
RD* Negated to Data Bus 3-Stated (Data Bus CL = 50 pF)	7			15	ns
RD*, WR* Rise/Fall Time	8			5	ns
Write Data Setup Time	9	35			ns
Write Data Hold Time	10	0			ns
Pixel and Control Data Setup Time	20	7			ns
Pixel and Control Data Hold Time	21	3			ns
CLOCK Cycle Time	22	25			ns
CLOCK Pulse Width High	23	7			ns
CLOCK Pulse Width Low	24	7			ns
CLOCK Rise/Fall Time (10% - 90%)	25			3	ns
Video Output Delay (CL = 10 pF)	26		20		ns
Video Output Rise/Fall Time (10% - 90%, CL = 10 pF)	27		3		ns
Video Output Settling Time (1 LSB, CL = 10 pF)	28		25		ns
Video Output Skew (CL = 10 pF)			0		ns
Video Pipeline Delay	29	2	2	2	CLOCK cycles
Glitch Energy (80 MHz, -3 db BW, CL = 10 pF)			50		pV - sec
DAC to DAC Crosstalk			100		pV - sec
Current Drain (VAA + VDD, f = 40 MHz)	IDD			200	mA

Test conditions: Unless otherwise specified, input values are 0.0 to 3.0 volts. All timing reference points are 1.5 volts for inputs, 50% for outputs. Input rise/fall times ≤ 2 ns. Output rise/fall time 10% - 90%.

Timing Waveforms



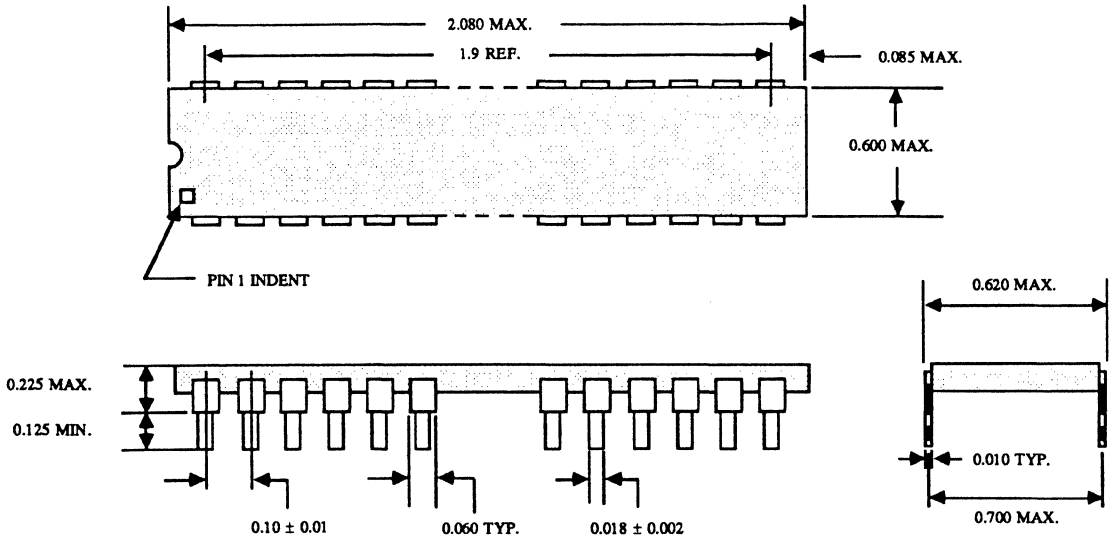
MPU Read/Write Timing.



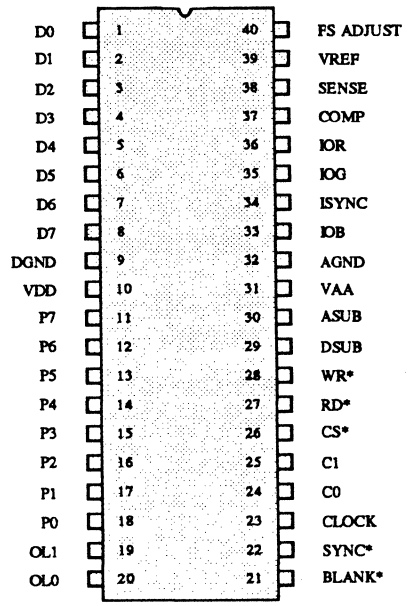
Video Input/Output Timing.

Packaging (Mechanical Data)

Notes: 1. Drawings are not to scale.
2. Units are in inches.



Pin Configuration



ORDERING INFORMATION				
Model Number	Speed	Screening	Package	Ambient Temperature Range
Bt453KC	40 MHz	Commercial	CERDIP	0° to +70° C.

CAUTION

ESD sensitive device. Permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

Do not insert this device into powered sockets. Remove power before insertion or removal.

Specifications are subject to change without notice.

DS014a-1/86

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580
TLX 383 596

Brooktree™

REV.	ZONE	ECO#	REVISION	APPD	DATE
A		R1244	PRODUCTION RELEASE		
B		R2195	REVISED PER ECN *M. MORI 7-10-90*		

NOTE:
MANUFACTURERS RECEIVING APPLE APPROVED VENDOR STATUS FOR THEIR PRODUCT UNDER THIS PART NUMBER PLEASE NOTE: You must not change your part design, materials or manufacturing process from those used for the original samples submitted to and approved by Apple without written approval of Apple. Proposed changes determined by Apple to be significant, will require the manufacturer to submit new samples and/or data for review and approval prior to product shipments to Apple.

	METRIC	**Apple Computer, Inc.**
DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN BRACKETS [ ] ARE IN INCHES. TOLERANCES X.X ± 0.3 [.01] X.XX ± 0.13 [.005] X.XXX ± 0.03 [.001] ANGLEs ± 0.1 or as noted DO NOT SCALE DRAWING	DRAFT V.M.V. 04/28/88 · DESIGN CK K.L. 04/27/88 ENG APPD Q.H. 04/27/88 · MFG APPD // QA APPD // · DESIGNER // RELEASE D.B. 08/25/88 · SCALE NONE MATERIAL/FINISH NOTED AS APPLICABLE · SIZE A	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART TITLE: IC, BROOKTREE Bt453, RAMDAC, 44-PIN PLCC DRAWING NUMBER 357S0003-B · SHT 1/16

1.0 SCOPE: This specifies the parametric requirements for a CMOS triple 8-bit video RAMDEC, 44-Pin PLCC package.

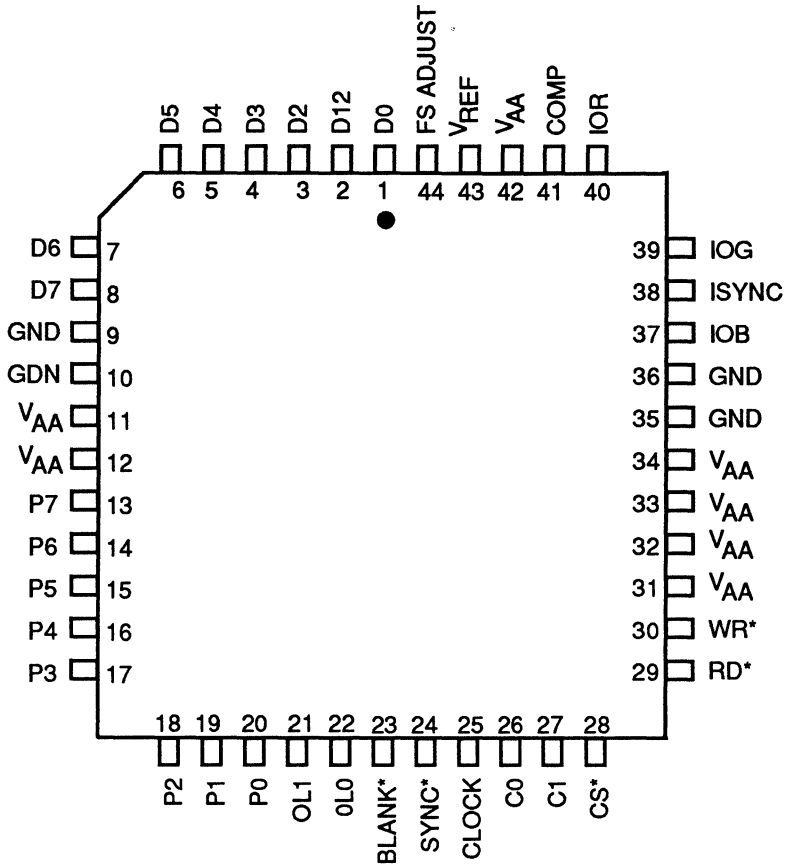


FIGURE 1. PIN CONFIGURATION

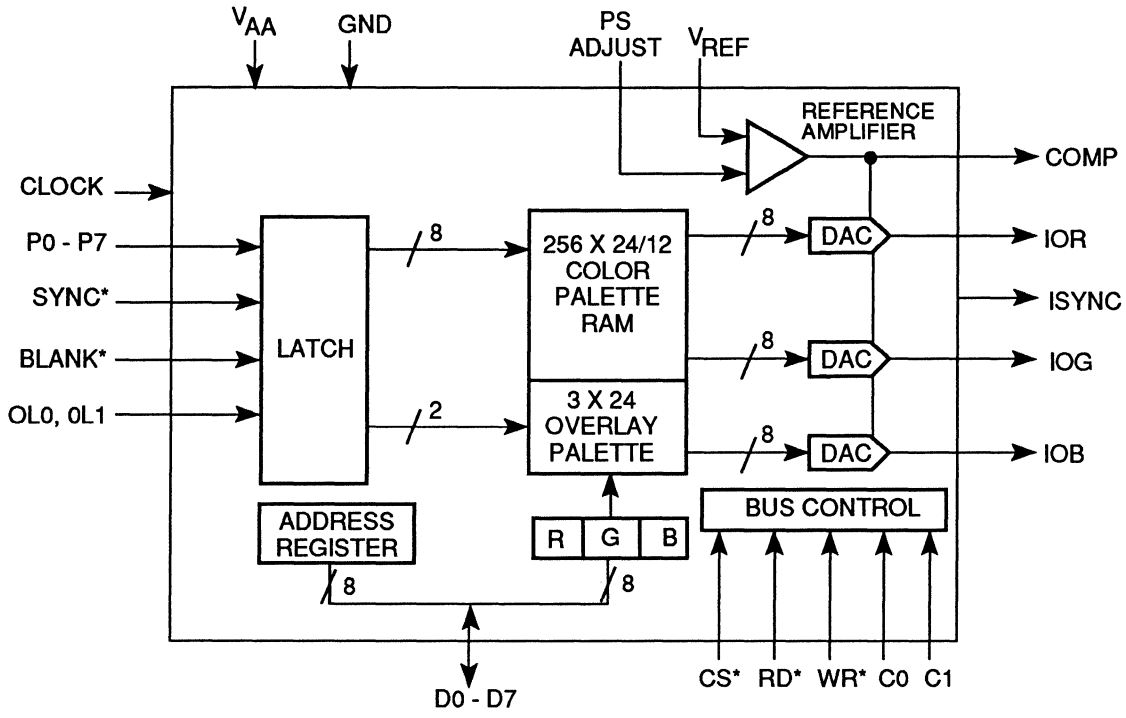


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	357S0003-B
SCALE: NONE	SHT 2 OF 16

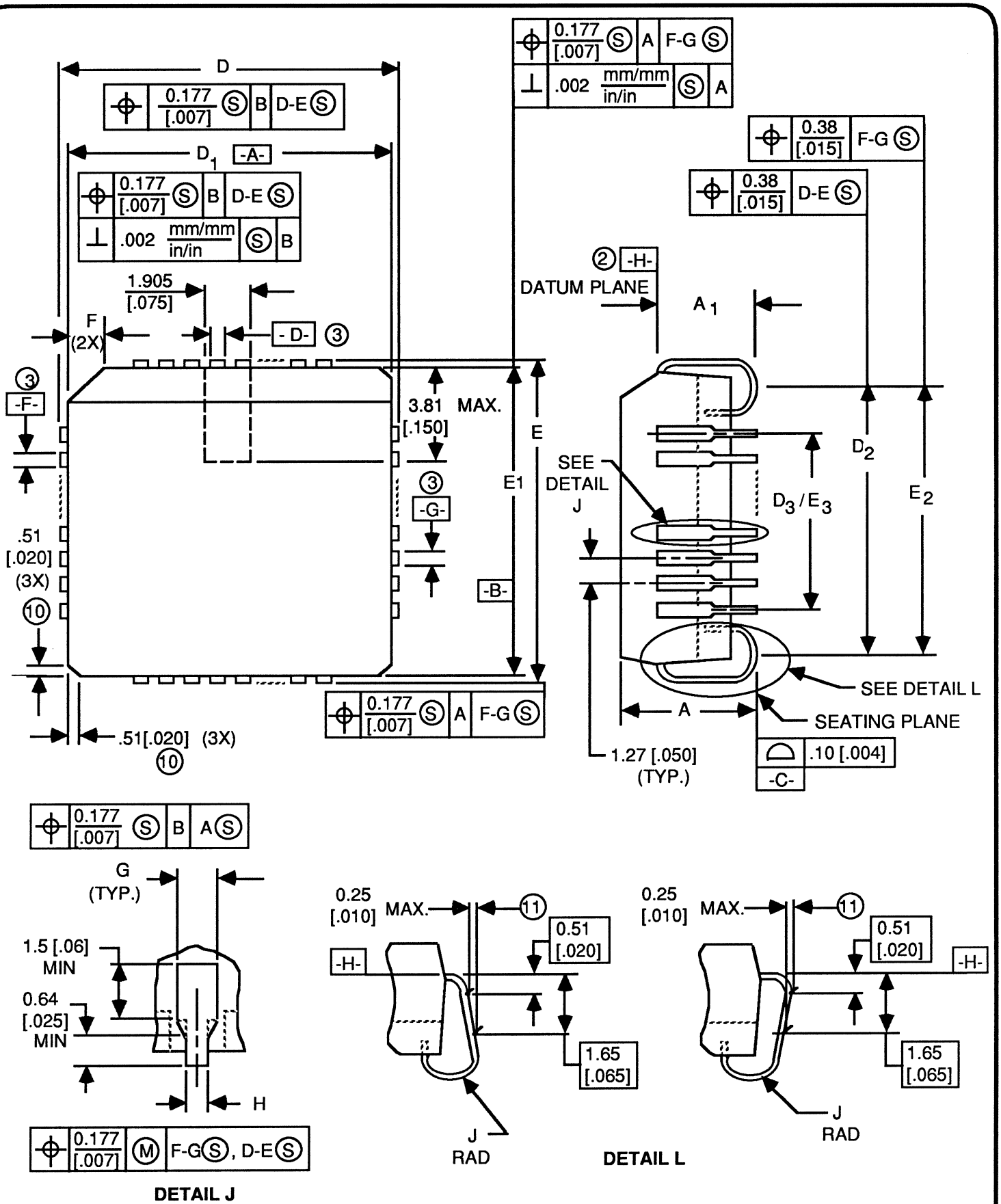


FIGURE 3. DIMENSIONS

Apple Computer, Inc.®

SIZE	DRAWING NUMBER
A	357S0003-B
SCALE: NONE	SHT 3 OF 16

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.57	0.165	0..180
A_1	2.29	3.04	0.090	0.120
D	17.40	17.65	0.685	0.695
D_1	16.51	16.62	0.650	0.656
D_2	14.99	16.00	0.590	0.630
D_3	12.70 REF.		0.500 REF.	
E	17.40	17.65	0.685	0.695
E_1	14.99	16.00	0.650	0.656
E_2	14.99	16.00	0.590	0.630
E_3	12.70 REF.		0.500 REF.	
F	1.07	1.22	0.042	0.048
G	0.66	0.81	0.026	0.032
H	0.33	0.53	0.013	0.021
J	0.64	1.14	0.025	0.045

PLCC-44

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS PLASTIC BODY.
3. DATUMS D-E AND F-G TO BE DETERMINED WHERE CENTER LEADS EXIT PLASTIC BODY AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLANE -C-.
5. TRANSITION IS OPTIONAL.
6. PLASTIC BODY DETAILS BETWEEN LEADS ARE OPTIONAL.
7. DIMENSIONS D_1 AND E_1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .254[.010].
8. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN ONE OFTHE ZONES INDICATED.
9. LOCATION TO DATUMS -A- AND -B- TO BE DETERMINED AT PLANE -H-.
10. EXACT SHAPE OF THIS FEATURE IS OPTIONAL.
11. THESE TWO DIMENSIONS DETERMINE MAXIMUM ANGLE OF THE LEAD FOR CERTAIN SOCKET APPLICATIONS. IF UNIT IS INTENDED TO BE SOCKETED, IT IS ADVISABLE TO REVIEW THESE DIMENSIONS WITH THE SOCKET SUPPLIER.
12. CONTROLLING DIMENSION: INCH.

FIGURE 3. DIMENSIONS (CONT)

2.0 APPLICABLE DOCUMENTS:

EIA RS-186 Standard test methods for passive components.
MIL-STD-883 Test methods and procedures for microelectronics.

3.0 REQUIREMENTS:

3.1 PHYSICAL:

3.1.1 PACKAGE: Void free plastic 40-pin PLCC package, with leads tin-lead plated. Dimensions per Figure 3. Pin configuration per Figure 1.

3.1.2 MARKINGS: Manufacturer's name or industry recognized logo, manufacturing date code, and manufacturer's or Apple's part number.

3.1.3 SOLDERABILITY: Leads solderability must meet EIA RS-186-9.

3.1.4 FUNCTIONAL BLOCK DIAGRAM: See Figure 2.

3.2 ELECTRICAL:

3.2.1 ELECTROSTATIC DISCHARGE SENSITIVITY: The minimum electrostatic discharge voltage per pin is ±2000 volts as specified in MIL-STD-883C, method 3015.3 (i.e., C = 100 pF, R = 1.5KΩ).

3.2.2 LATCH-UP TEST: The minimum latch-up current for all pins except ground is 50mA in both positive and negative directions. This applies to full temperature and power supply ranges.

3.2.3 OPERATING CONDITIONS: Per Table 2.

3.2.4 ABSOLUTE MAXIMUM RATINGS: Per Table 3.

3.2.5 STATIC PARAMETERS: Per Table 4.

3.2.6 DYNAMIC PARAMETERS: Per Table 5.

3.3 ENVIRONMENTAL:

3.3.1 RESISTANCE TO SOLDERING HEAT: 260°C for 10 sec in molten solder after 218°C for 30 sec in vapor phase, 60/40 solder and 260°C for 10 sec in molten solder after 240°C for 30 sec in I.R., 60/40 solder. Rate of temperature rise is 3°C/sec to within 100°C of the final temperature.

3.3.2 CLEANING: Parts must be washable in standard flux removal solvent and must not trap any cleaning liquids.

4.0 QUALITY ASSURANCE PROVISIONS:

Parts shall be inspected to assure compliance to the requirements of this document.

5.0 PACKAGING:

Parts shall be packaged according to requirements specified in purchase order for safe delivery at Apple or Apple designated contractor. (Parts requiring Tape & Reel shall meet the proper Tape & Reel specification per the purchase order.)

TABLE 1. PIN DESCRIPTIONS

PIN NAME	PIN NO.	DESCRIPTION
BLANK*	21	Composite blank control input (TTL compatible). A logic zero drives the IOR, IOG, and IOB outputs to the blanking level. as illustrated in Table 10. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	22	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 3). SYNC* does not override any other control or data input. as shown in Table 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	23	Clock input ('TTL computable). The rising edge of CLOCK latches the P0 - P7, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK by driven by a dedicated TTL buffer.
PO - P7	18,17,16, 15,14,13, 12,11	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	19,20	Overlay select inputs ('TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 9. When accessing the overlay palette, the P0 - P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	36,35,33	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable (Figure 8). All outputs, whether used or not, should have the same output load.
ISYNC	34	Sync current output. This high impedance current source is typically connected directly to the IOG output (Figure 8), and is used to encode sync information onto the green channel. ISYNC does not output any current while SYNC* is a logical zero. The amount of current output while SYNC* is a logical one is one is: ISYNC (mA) = 1,728 * VREF (V) / RSET Ω) If sync information is not required on the green channel, this output should be connected to GND.
FS ADJUST	40	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 8). Note that the IRE relationships in Figure 8 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is (assuming ISYNC is connected to IOG): IOG (mA) = (K + 326 + 1,728) * VREF (V) / RSET (Ω) The relationship between RSET and the full scale output current on IOR and IOB is: IOR, IOB (mA) = (K + 326) * VREF (V) / RSET (Ω) where K = 3,993 for the Bt453 and 3,760 for the Bt456. The difference is due to the fact that the Bt456 uses only the upper four bits of the DACs. Thus, for a given RSET value, the Bt456 will output slightly less gray scale current than the Bt453.

TABLE 1. PIN DESCRIPTIONS (Cont'd)

PIN NAME	PIN NO.	DESCRIPTION
COMP	37	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and V_{AA} (Figure 4).
V_{REF}	39	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.2v (typical) reference. The Bt4S31456 has an internal pull-up resistor between V_{REF} and V_{AA}. As the value of this resistor may vary slightly due to process variations, the use of a resistor divider network to generate the reference voltage is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to V_{AA}, as shown in Figure 4.
V_{AA}	10,29,30, 31,38	Analog power. All V_{AA} pins must be connected.
GND	9,32	Analog ground. All GND pins must be connected.
CS*	26	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. While CS* is a logical zero, the IOR, IOG, and IOB outputs are forced to the black Level. Note that the Bt453/456 will not function correctly while CS*, RD*, and WR* arc simultaneously a logical zero.
WR*	28	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 2.
RD*	27	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 2.
C0, C1	24,25	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed. as illustrated in Tables 6 and 7.
D0 - D7	1,2,3,4, 5,6,7,8	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

TABLE 2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{AA}	Power Supply	4.75	5.00	5.25	V
T_A	Ambient Operating Temperature	0		+ 70	°C
R_L	Output Load		37.5		Ω
V_{REF}	Reference Voltage	1.14	1.235	1.26	V
RSET	FS ADJUST Resistor		280		Ω

TABLE 3 ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
	V_{AA} (measured to GND)			7.0	V
	Voltage on any pin	GND-0.5		V_{AA} + 0.5	V
I_{SC}	Analog output short-circuit duration to any power supply or common		indefinite		
T_A	Ambient operating temperature	-55		+ 125	°C
T_{stg}	Storage temperature	-65		+ 150	°C
T_J	Junction temperature			+ 175	°C
T_{SOL}	Soldering temperature (5 seconds, 1/4 inch from pin)			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 4. D.C. CHARACTERISTIC

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
	Resolution (each DAC)	8	8	8	Bits
	Accuracy (each DAC)				
I_L	Integral Linearity	-1		+1	LSB
D_L	Differential Linearity	-1		+1	LSB
	Full Scale Error	-5		+5	% of FSR
	Zero Error	-5		+5	% of FSR
	Monotonicity		guaranteed		
	Coding				Binary
	Digital Inputs				
V_{IH}	Input High Voltage	2.0		V_{AA} + 0.5	V
V_{IL}	Input Low Voltage	DGND - 0.5		0.8	V
I_{IH}	Input High Current (Vin = 2.4v)			1	µA
I_{IL}	Input Low Current (Vin = 0.4v)			-1	µA
C_{IN}	Input Capacitance (f = 1 MHz, Vin = 2.4V)			10	pF
	Digital Outputs				
V_{OH}	Output High Voltage	2.4			V
V_{OL}	Output Low Voltage			0.4	V
I_{OL}	Output Low Current (VOL = 0.4V)	3.2			mA
I_{OH}	Output High Current (VOH = 2.4v)	400			µA
I_{OZ}	3-State Current			10	µA
C_{DO}	Output Capacitance			20	pF
	Analog Outputs				
	Gray Scale Current Range	15		22	mA
	Output Current				
	White Level Relative to Blank				
	Bt453	17.69	19.05	20.40	mA
	Bt456	16.70	18.02	19.31	mA
	White Level Relative to Black				
	Bt453	16.74	17.62	18.50	mA
	Bt456	15.75	16.58	17.41	mA
	Black Level Relative to Blank	0.95	1.44	1.90	mA
	Blank Level on IOR, IOB	0	5	50	µA
	Blank Level on IOG	6 .29	7 . 62	8 .96	mA
	Sync Level on IOG	0	5	50	µA
	LSB Size				
	Bt453		69.1		mA
	Bt4S6		1.105		mA
	DAC to DAC Matching		2	5	%

TABLE 4. D.C. CHARACTERISTIC (Cont'd)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{OC}	Output Compliance	- 1.0		+ 1.4	V
RAOUT	Output Impedance		10		KΩ
CAOUT	Output Capacitance (f = 1 MHz, IOUT = 0 mA)		30		pF
IREF	Voltage Reference Input Current		10		µA
PSRR	Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)		0.12	0.5	%/% ΔV_{AA}

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 ohms. VREF = 1.235v, ISYNC connected to IOG. Numbers in parentheses indicate Bt456 parameter value. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

TABLE 5. A. C. CHARACTERISTICS (Over recommended operating conditions)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fmax	Clock Rate			40	MHz
1	CS*, C0, C1 Setup Time	35			ns
2	CS*, C0, C1 Hold Time	35			ns
3	RD*, WR* High Time	25			ns
4	RD* Asserted to Data Bus Driven (Data Bus CL = 50pF)	10			ns
5	RD* Asserted to Data Valid (Data Bus CL = 50 pF)			100	ns
6	RD* Negated to data Bus 3-Stated (Data Bus CL = 50 pF)			15	ns
7	WR* Low Time	50			ns
8	Write Data Setup Time	35			ns
9	Write Data Hold Time	0			ns
10	Pixel and Control Setup Time	7			ns
11	Pixel and Control Hold Time	3			ns
12	CLOCK Cycle Time	25			ns
13	CLOCK Pulse Width High Time	7			ns
14	CLOCK Pulse Width Low Time	7			ns
15	Analog Output Delay		20	30	ns
16	Analog Output Rise/Fall Time		3		ns
17	Analog Output Settling Time		25		ns
	Analog Output Skew		1	2	ns
	Glitch Impulse*		50		pV - sec
18	Pipeline Delay	2	2	2	
I_{AA}	V_{AA} Current Drain**		190	250	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 ohms, VREF= 1.235v, ISYNC connected to IOG. TTL input values are 0 to 3 volts, with input rise/fall times < 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10pF, D0 - D7 output load ≤ 50 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. *Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k-ohm resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2 clock rate.

** at Fmax. I_{AA} (typ) at V_{AA} = 5.0v. I_{AA} (max) at V_{AA} = 5.25v.

TABLE 6 CONTROL INPUT TRUTH TABLE.

C1	C0	FUNCTION ADDRESSED BY MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

TABLE 7. ADDRESS REGISTER (ADDR) OPERATION.

		VALUE	C1	C0	ADDRESSES
ADDRa, b	counts modulo 3,	00 01 10			red value green value blue value
ADDR0-7	counts binary,	$00-$FF XXXX XX00 XXXX XX01 XXXX XX10 XXXX XX11	0 1 1 1 1	1 1 1 1 1	color palette RAM reserved overlay color 1 overlay color 2 overlay color 3

TABLE 8. TRUTH TABLE FOR MPU READ/WRITE OPERATIONS (CS*=0)

RD*	WR*	C0	ADDRb	ADDRa	FUNCTION
1	0	0	X	X	write address register; D0 - D7 —> ADDR0 - 7, 0 —> ADDR0a, ADDR0b
1	0	1	0	0	write red value; increment ADDRa - b
1	0	1	0	1	write green value; increment ADDRa - b
1	0	1	1	0	wriite blue value; modify location, increment ADDR0 - 7, increment ADDRa - b
0	1	0	X	X	read address register; ADDR2 - 7 —> D0 - D7
0	1	1	0	0	read red value; increment ADDRa- b
0	1	1	0	1	read green value; increment ADDRa - b
0	1	1	1	0	read blue value; increment ADDRO0 - 7, increment ADDRa - b
0	0	X	X	X	invalid operation

TABLE 9. PIXEL SELECT AND OVERLAY CONTROL TRUTH TABLE.

OL1	OL0	P7 - P0	ADDRESSES
0	0	$00	color palette RAM location $00
0	0	$01	color palette RAM location $01
.	.	.	.
.	.	.	.
0	0	$FF	color palette RAM location $FF
0	1	$xx	overlay color 1
1	0	$xx	overlay color 2
1	1	$xx	overlay color 3

TABLE 10. VIDEO OUTPUT TRUTH TABLE.

DESCRIPTION	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC INPUT DATA
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA -SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Typical with full scale IOG = 26.67 mA. RSET = 280 ohms, VREF = 1.235v.
ISYNC connected to IOG.
Note that the Bt456 uses only the upper four DAC input data bits.

6.0 SUPLEMENTAL INFORMATION: The following is not to be used for the acceptance nor rejection of the part herein.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the 453 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The MPU interface operates asynchronously to the video data. simplifying the design interface.
The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM, or the overlay registers, as shown in Table 6. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.
To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.
To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 bits cach of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay rcegisters. Following the blue read cycle, the address register increments to the next location which thc MPU may read by simply reading another sequence of red, green, and blue data.
Note that anytime the CS* input is a logical zero, the video outputs arc forced to the black level. When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay color registers, the address register increments following a blue read or write cycle However, while accessing the overlay color registers, the six most significant bits of the address register (ADDR2 - 7) are ignored.
To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb, that count modulo three, as shown in Tables 7 and 8. They arc reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0 - 7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers. as shown in Table 7. They are incremented following a blue read or write cycle, as shown in Table 8. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers.

Frame Buffer Interface

While CS* is a logical one, the P0- P7. OL0, and OL1 inputs are used to address the color palette RAM and overlay registers. as shown in Table 4. The addressed location provides 24 bits (12 bits for the Bt4S6) of color information to the three D/A converters.
The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 5 details how the SYNC* and BLANK* inputs modify the output levels.
The analog outputs of the Bt453 and Bt456 are capable of directly driving a 37.5-ohm load, such as a doubly-terminated 75-ohm coaxial cable.

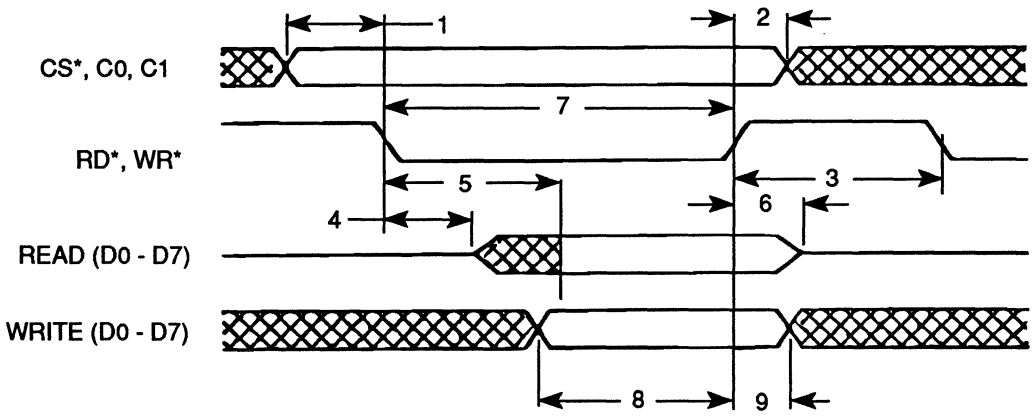
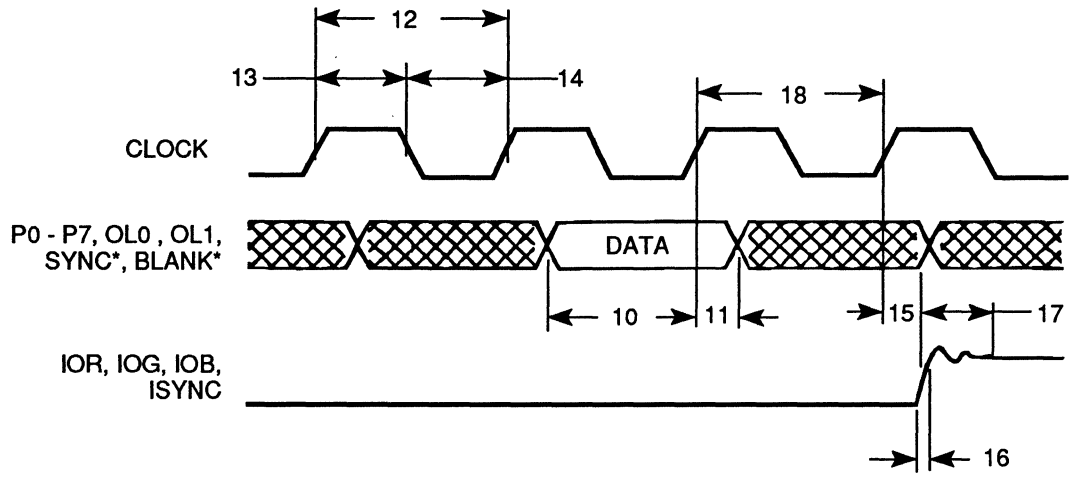


FIGURE 4. MPU READ/WRITE TIMING



Note
4. Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
5. Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB for the Bt453 or ± 1/8 LSB for the Bt456
6. Output rise/fall time measured between the 10% and 90% points of full scale transition.

FIGURE 5. VIDEO INPUT/OUTPUT TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	357S0003-B
SCALE: NONE	SHT 14 OF 16

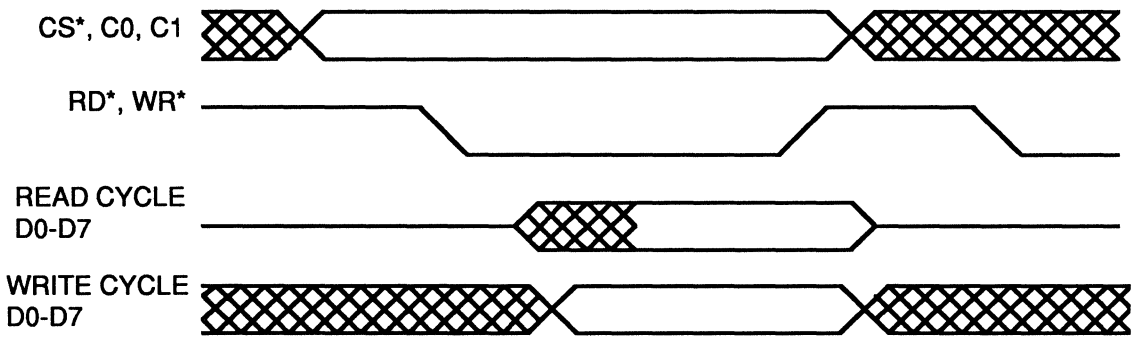


FIGURE 6. HOST MPU READ/WRITE TIMING

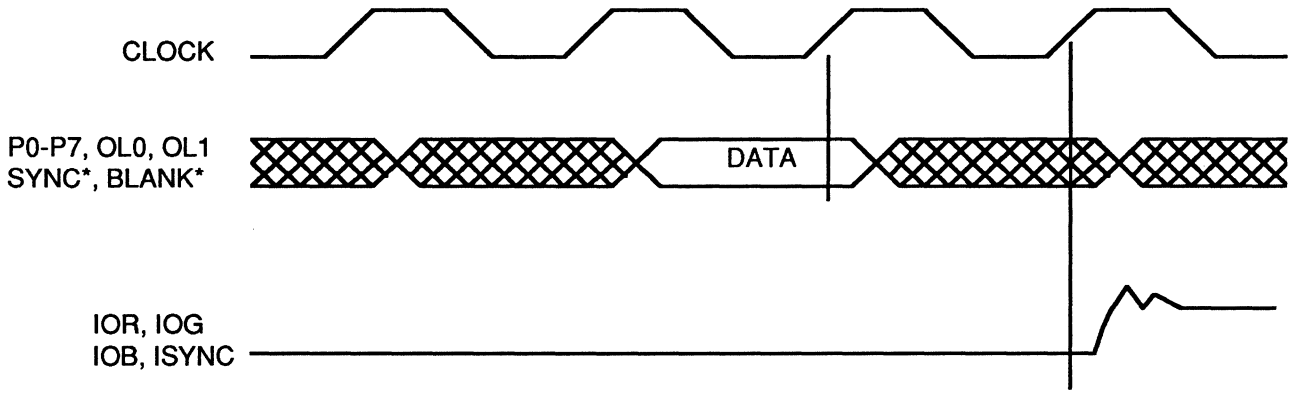
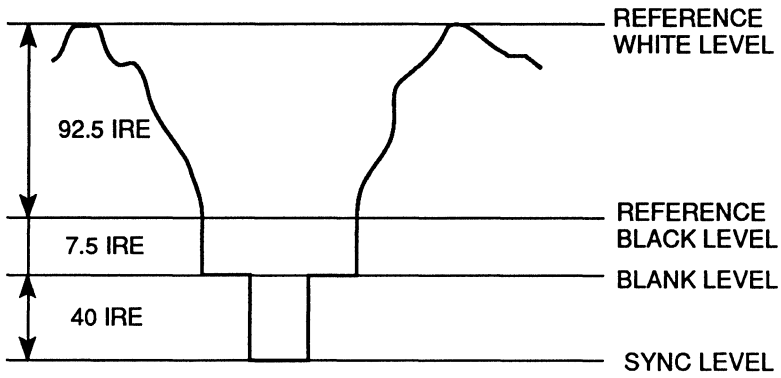


FIGURE 7. VIDEO INPUT/OUTPUT TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	357S0003-B
SCALE: NONE	SHT 15 OF 16

RED, BLUE		GREEN	
MA	V	MA	V
19.50	0.714	26.67	1.000
1.44	0.054	9.05	0.34
0.00	0.000	7.62	0.286
		0.00	0.000



NOTE:

75Ω doubly-terminated load, 528Ω, RS-343-A levels and tolerances assumed on all levels.

FIGURE 8. COMPOSITE VIDEO OUTPUT WAVEFORMS

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 357S0003-B | SCALE: NONE | SHT 16 OF 16