

NOTE:

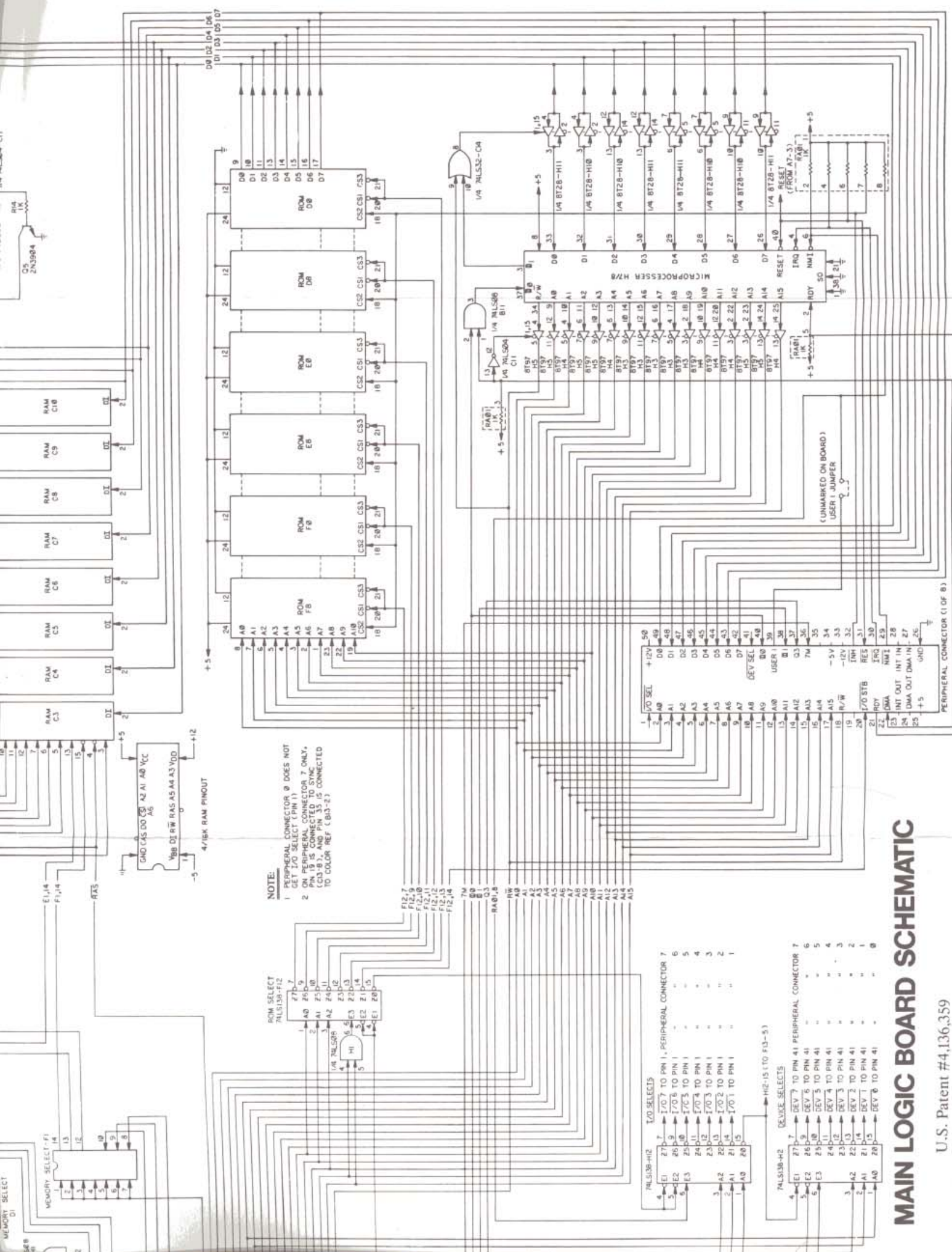
- PERIPHERAL CONNECTOR 8 DOES NOT GET I/O SELECT (PIN 1).
- ON PERIPHERAL CONNECTOR 7 ONLY, PIN 19 IS CONNECTED TO SYNC CDS-B, AND PIN 35 IS CONNECTED TO COLOR REF (BI3-2).

74LS139-H2	I/O SELECTS	PERIPHERAL CONNECTOR 7
4	E1	1/0 7 TO PIN 1, PERIPHERAL CONNECTOR 7
5	E2	1/0 6 TO PIN 1
6	E3	1/0 5 TO PIN 1
7	E4	1/0 4 TO PIN 1
8	E5	1/0 3 TO PIN 1
9	E6	1/0 2 TO PIN 1
10	E7	1/0 1 TO PIN 1
11	E8	1/0 0 TO PIN 1

74LS139-H2	DEVICE SELECTS	PERIPHERAL CONNECTOR 7
4	E1	DEV 7 TO PIN 41
5	E2	DEV 6 TO PIN 41
6	E3	DEV 5 TO PIN 41
7	E4	DEV 4 TO PIN 41
8	E5	DEV 3 TO PIN 41
9	E6	DEV 2 TO PIN 41
10	E7	DEV 1 TO PIN 41
11	E8	DEV 0 TO PIN 41

MAIN LOGIC BOARD SCHEMATIC

U.S. Patent #4,136,359



NOTE:

- 1 PERIPHERAL CONNECTOR 0 DOES NOT GET L/O SELECT (PIN 1)
- 2 ON PERIPHERAL CONNECTOR 7 ONLY, PIN 19 IS CONNECTED TO SYNC (CD3-B), AND PIN 35 IS CONNECTED TO COLOR REF (B03-2)

ROM SELECT
74LS138-F1

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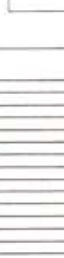
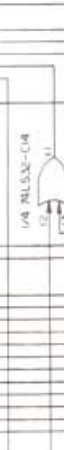
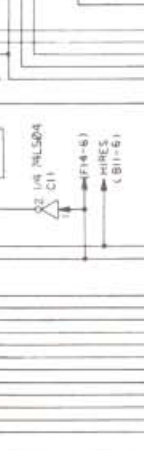
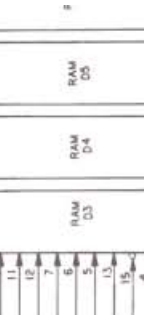
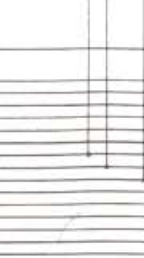
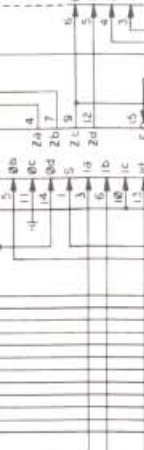
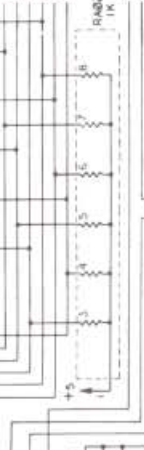
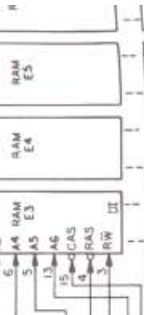
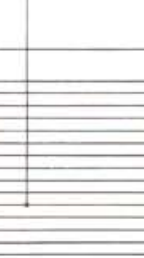
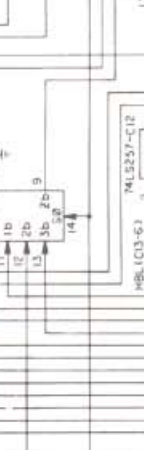
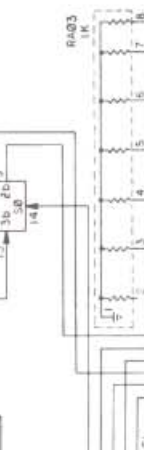
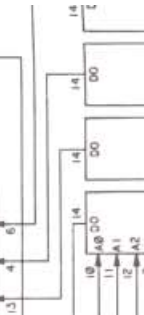
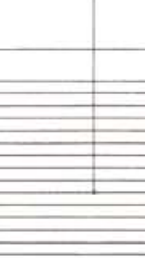
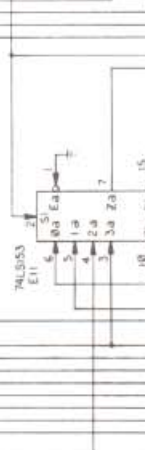
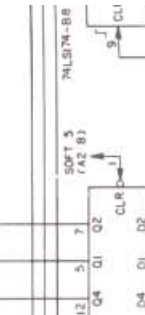
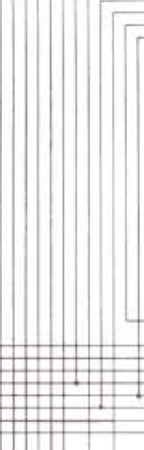
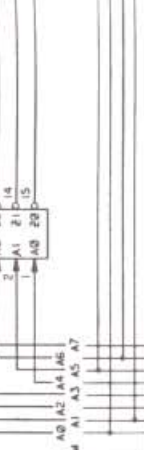
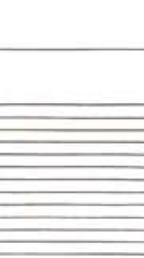
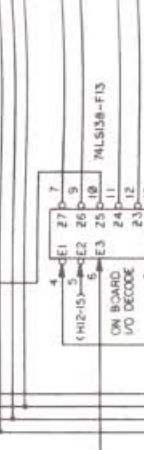
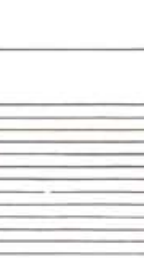
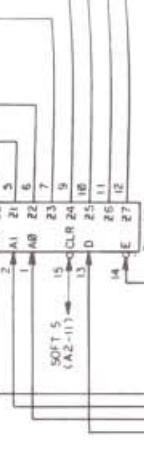
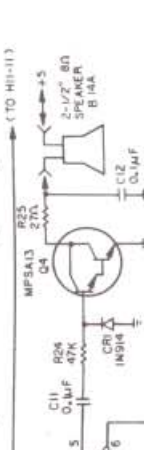
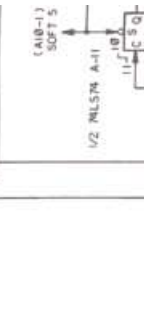
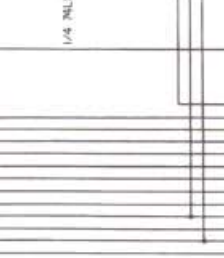
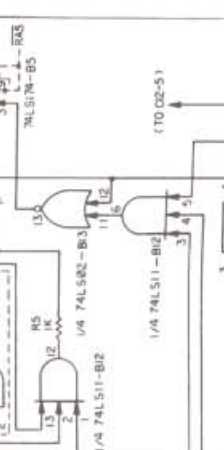
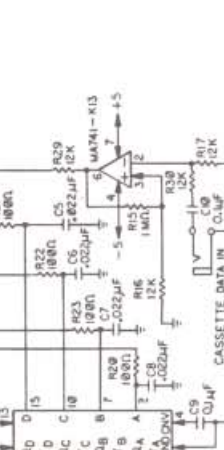
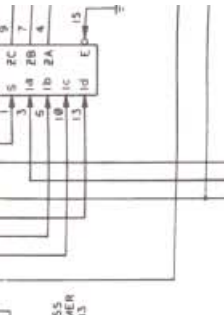
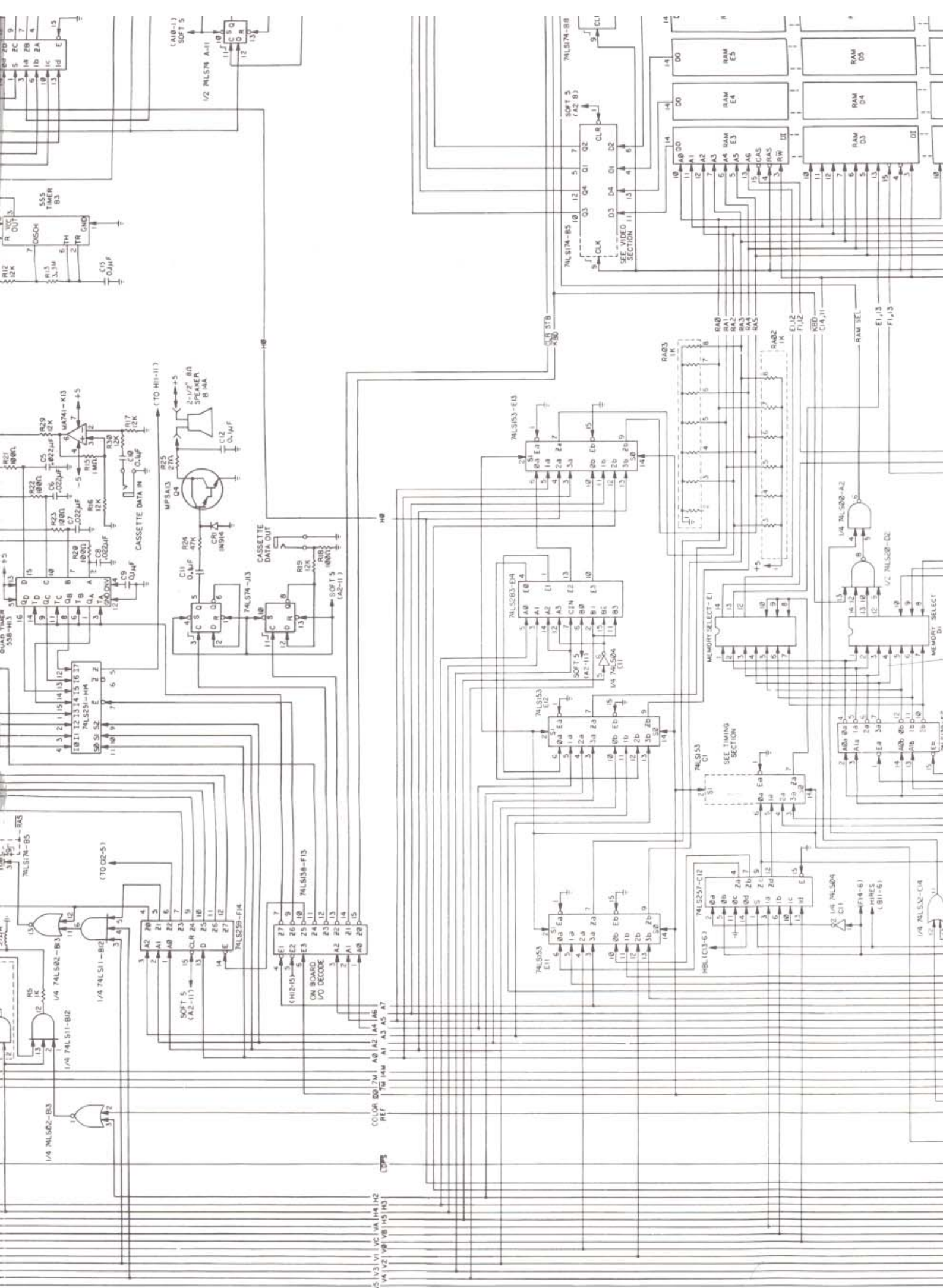
T/O SELECTS

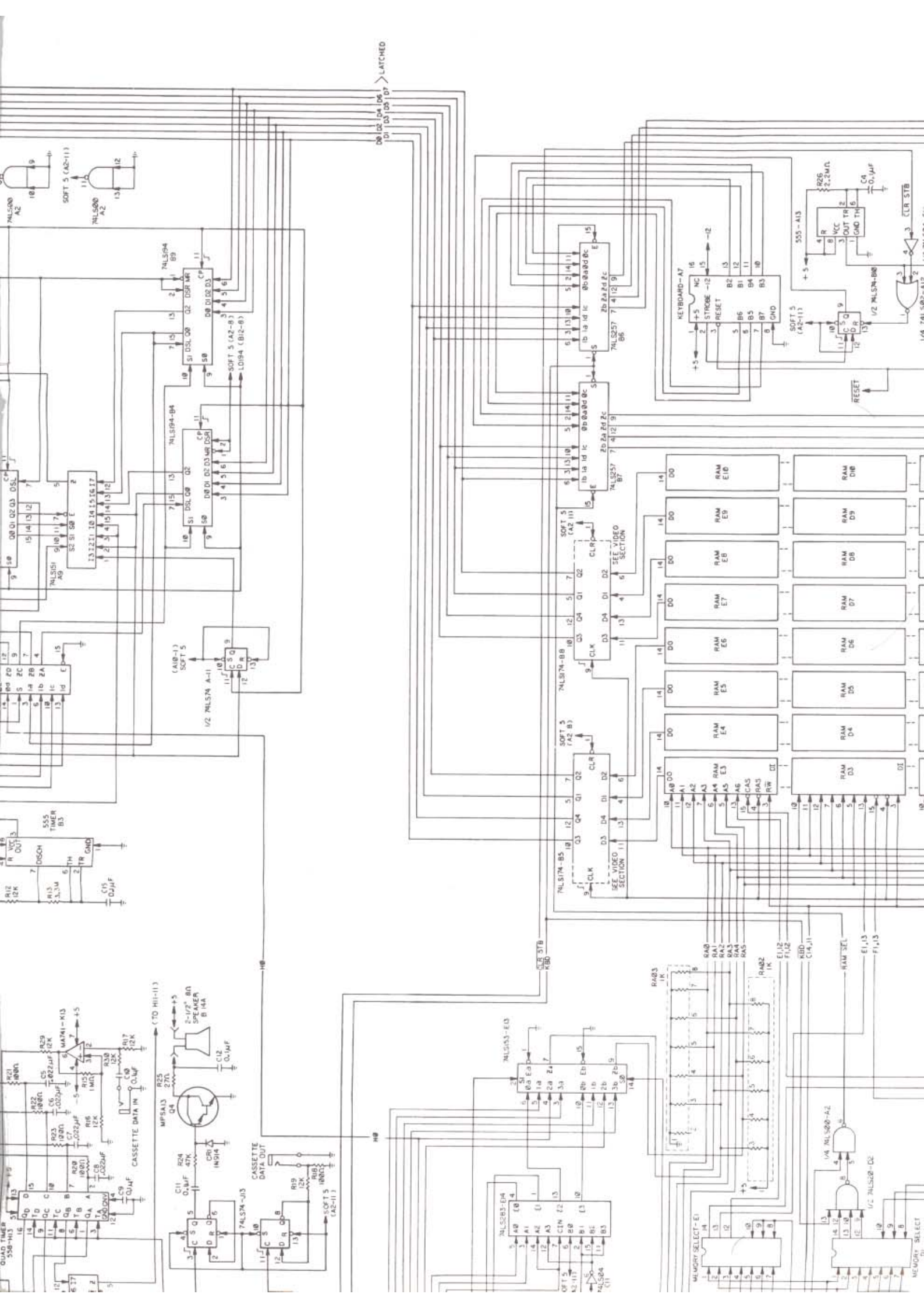
4	E1	27	7	I/O 7 TO PIN 1, PERIPHERAL CONNECTOR 7
5	E2	28	8	I/O 8 TO PIN 1
6	E3	29	9	I/O 9 TO PIN 1
		30	10	I/O 10 TO PIN 1
		31	11	I/O 11 TO PIN 1
		32	12	I/O 12 TO PIN 1
		33	13	I/O 13 TO PIN 1
		34	14	I/O 14 TO PIN 1
		35	15	I/O 15 TO PIN 1
		36	16	I/O 16 TO PIN 1
		37	17	I/O 17 TO PIN 1
		38	18	I/O 18 TO PIN 1
		39	19	I/O 19 TO PIN 1
		40	20	I/O 20 TO PIN 1
		41	21	I/O 21 TO PIN 1
		42	22	I/O 22 TO PIN 1
		43	23	I/O 23 TO PIN 1
		44	24	I/O 24 TO PIN 1
		45	25	I/O 25 TO PIN 1
		46	26	I/O 26 TO PIN 1
		47	27	I/O 27 TO PIN 1
		48	28	I/O 28 TO PIN 1
		49	29	I/O 29 TO PIN 1
		50	30	I/O 30 TO PIN 1

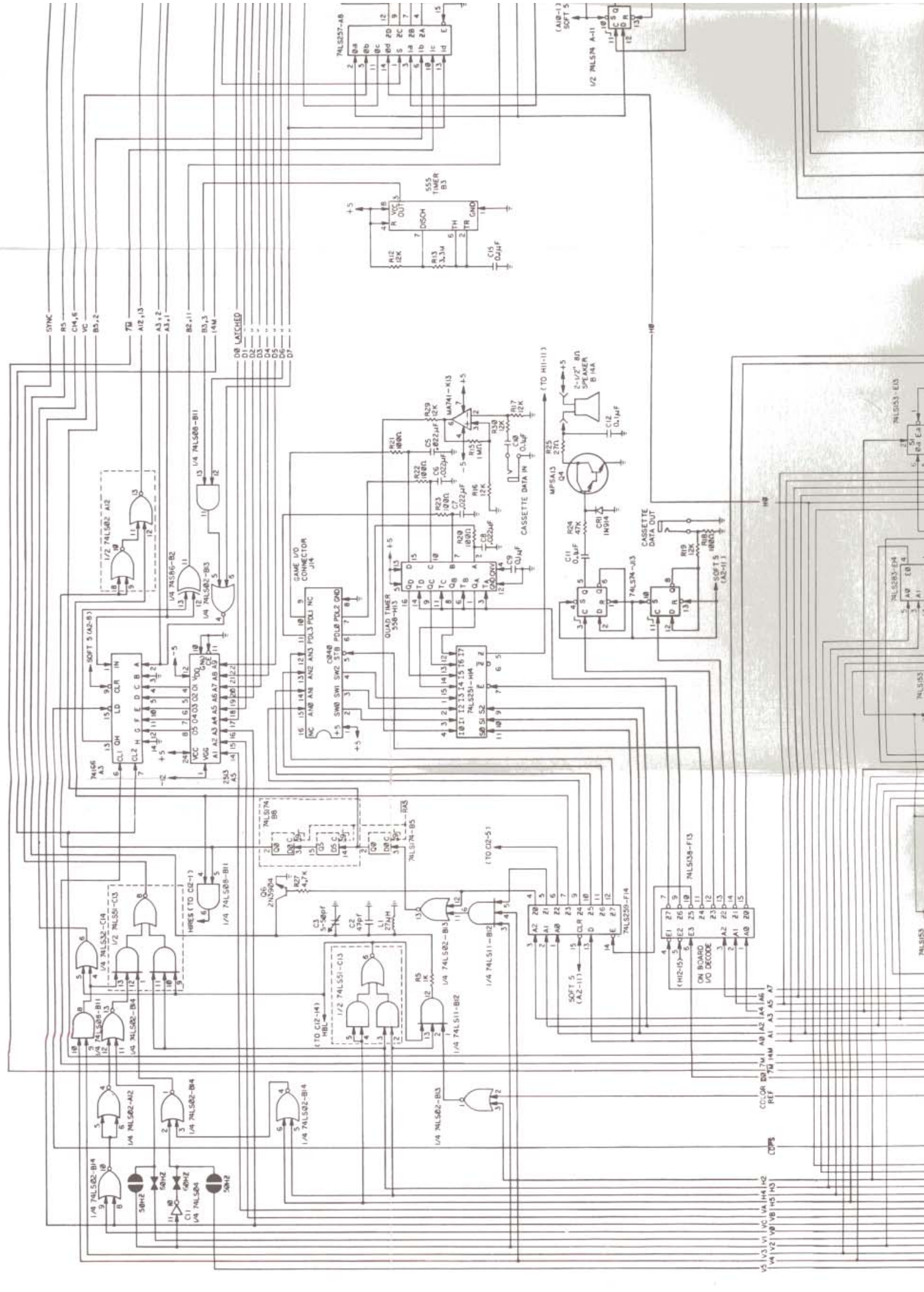
74LS138-H2 DEVICE SELECTS

4	E1	27	7	DEV 7 TO PIN 41 PERIPHERAL CONNECTOR 7
5	E2	28	8	DEV 8 TO PIN 41
6	E3	29	9	DEV 9 TO PIN 41
		30	10	DEV 10 TO PIN 41
		31	11	DEV 11 TO PIN 41
		32	12	DEV 12 TO PIN 41
		33	13	DEV 13 TO PIN 41
		34	14	DEV 14 TO PIN 41
		35	15	DEV 15 TO PIN 41
		36	16	DEV 16 TO PIN 41
		37	17	DEV 17 TO PIN 41
		38	18	DEV 18 TO PIN 41
		39	19	DEV 19 TO PIN 41
		40	20	DEV 20 TO PIN 41
		41	21	DEV 21 TO PIN 41
		42	22	DEV 22 TO PIN 41
		43	23	DEV 23 TO PIN 41
		44	24	DEV 24 TO PIN 41
		45	25	DEV 25 TO PIN 41
		46	26	DEV 26 TO PIN 41
		47	27	DEV 27 TO PIN 41
		48	28	DEV 28 TO PIN 41
		49	29	DEV 29 TO PIN 41
		50	30	DEV 30 TO PIN 41

MAIN LOGIC BOARD SCHEMATIC

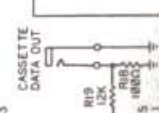
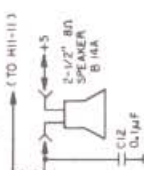
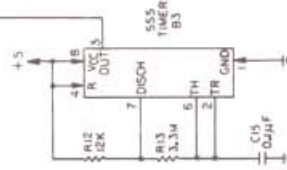






SYNC
R5
C14,6
VC
B5,2
7A
A12,13
A3,2
A3,1
B2,11
B5,3
14M

08 LATCHED
D1
D2
D3
D4
D5
D6
D7



ON BOARD I/O DECODE
(H2-15)
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
E19
E20

COLOR B0,7,4, A0, A2, A4, A6
REF 7,0, 14, M, A1, A3, A5, A7
C0, P5

U5, U3, U1, U0, U4, U4, U2
U4, U2, U0, U3, U5, U3, U5

