INTRODUCTION

The CCS 7811B Arithmetic Processor Unit is a powerful floating-point hardware unit which will significantly improve the execution speed of your APPLESOFT II programs. Program execution speeds can be increased by as much as an order of magnitude, depending on how much arithmetic a given program performs, and more sophisticated high-resolution graphics can be produced.

Whenever a speed advantage can be realized, the on-board arithmetic processor performs the APPLESOFT II operations and functions: multiplication, division, the trig functions, inverse tangents, square roots, exponentiation, and natural logarithms. To help you achieve the full power of the 7811B APU, additional functions have been created and are available through the use of the USR(x) function. These include arcsin and arccos of x, the log10 of x, the hyperbolic trig functions, the inverse of x, and pi.

Gaining this increased execution speed involves certain trade-offs. APPLESOFT maintains 8 or 9 significant digits, whereas the 7811B maintains 6 or 7. APPLESOFT gives you a range of approximately $10^{\pm 40}$, while the 7811B's range is approximately $10^{\pm 20}$. Finally, the 7811B truncates results, whereas APPLESOFT rounds them off. As a result, the slight errors inherent in digital computing will accumulate differently with the 7811B than with APPLESOFT. In most situations the improved speed offered by the 7811B will more than make up for the slight decrease in accuracy.

The 7811B with disk-loaded CCSOFT software is compatible as-is with standard APPLESOFT software. If you have an APPLESOFT ROM Card or APPLE II+, you will need to install a CCSOFT ROM, available separately from CCS. Installation instructions are included as Appendix A of this manual.
SUMMARY OF FEATURES

Uses an AM9511A Arithmetic Processor to Significantly Increase Execution Speeds of APPLESOFT II Arithmetic Operations and Derived Trigonometric and Algebraic Functions

Provides Additional Derived Functions through USR(x)

Provides 32-bit Binary Floating Point and 16-bit or 32-bit Fixed Point Data Formats

Converts Floating Point to Fixed Point and Fixed Point to Floating Point

Supports Interrupt Daisy Chain

Allows DMA Daisy Chain Pass-through

Provides Space for 256-byte Memory Add-on

Uses Glass Epoxy PC Board, Solder-Masked on Both Sides, with Component Silkscreen and Gold-Plated Connectors
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CHAPTER 1

THEORY OF OPERATION

The CCS 7811B, consisting of an AMD AM9511A Arithmetic Processor and the circuitry needed to successfully interface it with the APPLE II, provides high-performance fixed-point and floating-point arithmetic and a variety of floating-point mathematical and trigonometric functions. The specific operations and functions performed are listed in section 1.3 at the end of this chapter. An understanding of the following terms is assumed throughout this manual.

PRECISION: The number of distinct values an operand can represent is a function of its precision. For fixed point data, single-precision refers to 16-bit operands, double-precision to 32-bit operands.

FIXED POINT: The fixed point representation of an operand is a standard binary two's-complement value. The sign (positive=0) is located in the most significant bit (MSB). The range is \(-32,768\) to \(+32,767\) for single-precision and \(-2,147,483,648\) to \(+2,147,483,647\) for double-precision.

FLOATING POINT: The floating point format is analogous to scientific notation; it consists of a mantissa and an exponent expressed in 32 bits. The mantissa is located in the lower 24 bits. The binary point is to the left of bit 23, the MSB, which must be 1.
THEORY OF OPERATION

unless the value represented is Zero (which is represented by all 0’s). The exponent is represented by bits 24-29. Bit 30 is the exponent sign, bit 31 the mantissa sign (positive=0).

1.1 9511A OPERATION

To perform the operations and derive the functions listed in Section 1.3, the 9511A must be given data, then must be given a command telling it what to do with the data. Data is written to an internal, 16-bit-wide operand stack from which the Arithmetic Logic Unit receives the first operand for an operation. The second operand is supplied from the internal 16-bit bus. The least significant byte of an operand must be pushed onto the operand stack first.

The block diagram below shows the relationships of the main functional parts of the 9511A. The command byte comes across the data bus
THEORY OF OPERATION

to the Command Register, from which the Microprogram Controller reads it. The microprogram that controls the execution of the command is contained in the Control ROM. The Microprogram Controller causes the program instructions to be sent to the ALU, which carries out the necessary operations. Intermediate results are stored by the ALU in the Working Registers. The constants needed by the ALU to perform the mathematical operations (using Chebyshev Polynomials to minimize and distribute errors) are stored in the Constant ROM. Final results are popped onto the data lines most-significant-byte first.

The 9511A uses the inputs C/-D (Control/-Data), -WR, and -RD to determine the kind of transfer taking place. If C/-D is low, data is either popped from the operand stack onto the data bus (-RD low) or pushed from the data bus onto the stack (-WR low). If C/-D is high, a command is pushed from the data bus into the command register (-WR low), or the status byte is popped from the status register onto the data bus (-RD low).

<table>
<thead>
<tr>
<th>C/D</th>
<th>RD</th>
<th>WR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>PUSH DATA BYTE</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>POP DATA BYTE</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>ENTER COMMAND BYTE</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>READ STATUS</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>L</td>
<td>UNDEFINED</td>
</tr>
</tbody>
</table>

1-3
THEORY OF OPERATION

Command bytes for the AM9511A have the following format:

```
SVREQ  PRECISION  FORMAT  OPERATION CODE
```

Bits 0-4 select the operation to be performed. The data format is specified in bit 5: 0 for floating point, 1 for fixed point. Bit 6 controls the precision of the data for fixed point commands, a 1 specifying single-precision (16-bit) operands, a 0 specifying double-precision (32-bit) operands. All floating point operations use 32-bit operands, so if bit 5 is 0, bit 6 must be 0. Results are undefined for all illegal combinations of bits in the command byte.

A 1 in bit 7 causes the 9511A to output a service request after executing the command specified by bits 0-4. Since the 7811B does not use the SVREQ line from the 9511A to communicate with the computer, bit 7 will always be 0.

Status bytes have the following format:

```
BUSY  SIGN  ZERO  ERROR CODE  CARRY
```

If bit 1 is a 1, the previous operation resulted in a carry or borrow from the most significant bit. Bits 4-1 designate errors according to the following codes:

- 0000—No error
- 1000—Division by zero
- 0100—Square root or log of negative number
- 1100—Argument of ACOS, ASIN, or EXP too large
- xx10—Underflow
- xx01—Overflow

1-4
Bit 5 is a 1 if the value on the top of the stack is zero and Bit 6 is 1 if it is negative. If Bit 7 is a 1, the 9511A is executing a command.

1.2 SUPPORT CIRCUITRY

Eight bi-directional data lines are used for the transfer of data and instructions to and from the 9511A. An 8304B bi-directional line buffer drives the data lines with sufficient power to ensure successful data transfer, but in doing so consumes significant amounts of power. As the driver is not in use most of the time, we have provided a power-down feature. A transistor monitors the output of the flip-flop controlled by -DEV SEL, turning on power for the 8304B only when -DEV SEL has gone active. The direction of transfer through the 8304B is controlled by the R/-W line. The rest of the circuitry is used to let the 9511A know what to do with incoming data bytes and to let the CPU know when the 9511A has completed an operation.

The -RD and -WR inputs of the 9511A are controlled by the R/-W and -DEV SEL lines from the APPLE. The R/-W line is inverted and NANDed with -DEV SEL to control -WR; uninvited, it is NANDed with -DEV SEL to control -RD. The C/-D input is controlled directly by address line A0, and the -CS (Chip Select) input is controlled by -DEV SEL.

Because -DEV SEL remains valid for only half of one clock cycle and the 9511A requires that the inputs to -WR, -RD, and -CS remain valid longer than this (how long depends on the function being performed), the 7811B includes circuitry designed to maintain the -DEV SEL signal as long as the 9511A needs it. This is accomplished through the use of a D-type flip-flop which is clocked by -DEV SEL. The 9511A also requires that -RD and -WR be stable before -CS goes active. A sufficient delay is accomplished by taking the -CS input from the output of the data buffer transistor, which is controlled by the Device Select flip-flop.

The 7811B does not need on-board memory, but sockets are provided for users who wish to add 256 bytes of RAM or ROM. For ROM users, a power-down
THEORY OF OPERATION

feature is included to disable the ROMs when not in use. The W inputs are permanently disabled. RAM users must connect the RAM jumper. This disables the power-down feature (which would otherwise destroy the contents of the RAM) and allows the RAM's W inputs to be controlled by the R/W line.

The 7811B supports the interrupt daisy chain and allows DMA daisy chain pass-through. If the INT jumper is not connected, the interrupt daisy chain merely passes through the board: INT IN controls INT OUT. If the jumper is connected, a low -END output from the 9511A (signifying that the 9511A has completed execution of a command) pulls INT OUT low, disabling lower-priority interrupts. The inverted -END output is NANDed with INT IN to control the -IRQ line. An interrupt request is thus generated by the 7811B when -END goes low and INT IN is high (no higher-priority board generating an interrupt request).
THEORY OF OPERATION

1.3 9511A COMMAND SUMMARY

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>DESCRIPTION</th>
<th>CYCLES</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SINGLE-PRECISION FIXED POINT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SADD</td>
<td>Add TOS to NOS</td>
<td>16-18</td>
<td>6C</td>
</tr>
<tr>
<td>SSUB</td>
<td>Subtract TOS from NOS</td>
<td>30-32</td>
<td>6D</td>
</tr>
<tr>
<td>SMUL</td>
<td>Multiply NOS by TOS; Lower result</td>
<td>84-94</td>
<td>6E</td>
</tr>
<tr>
<td>SMUU</td>
<td>Multiply NOS by TOS; Upper result</td>
<td>80-98</td>
<td>76</td>
</tr>
<tr>
<td>SDIV</td>
<td>Divide NOS by TOS</td>
<td>84-94</td>
<td>6F</td>
</tr>
<tr>
<td><strong>DOUBLE-PRECISION FIXED POINT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDAD</td>
<td>Add TOS to NOS</td>
<td>20-22</td>
<td>2C</td>
</tr>
<tr>
<td>DSUB</td>
<td>Subtract TOS from NOS</td>
<td>38-40</td>
<td>2D</td>
</tr>
<tr>
<td>DMUL</td>
<td>Multiply NOS by TOS; Lower</td>
<td>194-210</td>
<td>2E</td>
</tr>
<tr>
<td>DMUU</td>
<td>Multiply NOS by TOS; Upper</td>
<td>182-218</td>
<td>36</td>
</tr>
<tr>
<td>DDIV</td>
<td>Divide NOS by TOS</td>
<td>196-210</td>
<td>2F</td>
</tr>
<tr>
<td><strong>FLOATING POINT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FADD</td>
<td>Add TOS to NOS</td>
<td>54-368</td>
<td>10</td>
</tr>
<tr>
<td>FSUB</td>
<td>Subtract TOS from NOS</td>
<td>70-370</td>
<td>11</td>
</tr>
<tr>
<td>FMUL</td>
<td>Multiply NOS by TOS</td>
<td>146-168</td>
<td>12</td>
</tr>
<tr>
<td>FDIV</td>
<td>Divide NOS by TOS</td>
<td>154-184</td>
<td>13</td>
</tr>
<tr>
<td><strong>DERIVED FLOATING POINT FUNCTIONS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SQRT</td>
<td>Square Root of TOS</td>
<td>782-870</td>
<td>01</td>
</tr>
<tr>
<td>SIN</td>
<td>Sine of TOS</td>
<td>3796-4808</td>
<td>02</td>
</tr>
<tr>
<td>COS</td>
<td>Cosine of TOS</td>
<td>3840-4878</td>
<td>03</td>
</tr>
<tr>
<td>TAN</td>
<td>Tangent of TOS</td>
<td>4894-5886</td>
<td>04</td>
</tr>
<tr>
<td>ASIN</td>
<td>Inverse Sine of TOS</td>
<td>6230-7938</td>
<td>05</td>
</tr>
<tr>
<td>ACOS</td>
<td>Inverse Cosine of TOS</td>
<td>6304-8284</td>
<td>06</td>
</tr>
<tr>
<td>ATAN</td>
<td>Inverse Tangent of TOS</td>
<td>4992-6536</td>
<td>07</td>
</tr>
<tr>
<td>LOG</td>
<td>Common Logarithm of TOS</td>
<td>4474-7132</td>
<td>08</td>
</tr>
<tr>
<td>LN</td>
<td>Natural Logarithm TOS</td>
<td>4298-6956</td>
<td>09</td>
</tr>
<tr>
<td>EXP</td>
<td>(e) raised to power in TOS</td>
<td>3794-4878</td>
<td>0A</td>
</tr>
<tr>
<td>PWR</td>
<td>NOS raised to power in TOS</td>
<td>8290-12032</td>
<td>0B</td>
</tr>
<tr>
<td><strong>DATA MANIPULATION COMMANDS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOP</td>
<td>No operation</td>
<td>4</td>
<td>00</td>
</tr>
<tr>
<td>FIXS</td>
<td>Convert TOS from FP to SP format</td>
<td>90-214</td>
<td>1F</td>
</tr>
<tr>
<td>FIXD</td>
<td>Convert TOS from FP to DP format</td>
<td>90-336</td>
<td>1E</td>
</tr>
<tr>
<td>FLTS</td>
<td>Convert TOS from SP to FP format</td>
<td>62-156</td>
<td>1D</td>
</tr>
<tr>
<td>FLTD</td>
<td>Convert TOS from DP to FP format</td>
<td>56-342</td>
<td>1C</td>
</tr>
<tr>
<td>CHSS</td>
<td>Change sign of SP operand to TOS</td>
<td>22-24</td>
<td>74</td>
</tr>
<tr>
<td>CHSD</td>
<td>Change sign of DP operand to TOS</td>
<td>26-28</td>
<td>34</td>
</tr>
<tr>
<td>CHSF</td>
<td>Change sign of FP operand to TOS</td>
<td>16-20</td>
<td>15</td>
</tr>
</tbody>
</table>
### THEORY OF OPERATION

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>Code 1</th>
<th>Code 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTOS</td>
<td>Push SP operand on TOS to NOS</td>
<td>16 77</td>
<td></td>
</tr>
<tr>
<td>PTOD</td>
<td>Push DP operand on TOS to NOS</td>
<td>20 37</td>
<td></td>
</tr>
<tr>
<td>PTOF</td>
<td>Push FP operand on TOS to NOS</td>
<td>20 17</td>
<td></td>
</tr>
<tr>
<td>POPS</td>
<td>Pop SP operand from TOS</td>
<td>10 78</td>
<td></td>
</tr>
<tr>
<td>POPD</td>
<td>Pop DP operand from TOS</td>
<td>12 38</td>
<td></td>
</tr>
<tr>
<td>POPF</td>
<td>Pop FP operand from TOS</td>
<td>12 18</td>
<td></td>
</tr>
<tr>
<td>XCHS</td>
<td>Exchange SP operands TOS and NOS</td>
<td>18 79</td>
<td></td>
</tr>
<tr>
<td>XCHD</td>
<td>Exchange DP operands TOR and NOS</td>
<td>26 39</td>
<td></td>
</tr>
<tr>
<td>XCHF</td>
<td>Exchange FP operands TOS and NOS</td>
<td>26 19</td>
<td></td>
</tr>
<tr>
<td>PUPI</td>
<td>Push FP constant PI to TOS</td>
<td>16 1A</td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:

1. **ABBREVIATIONS:**
   - TOS = Top of Stack
   - NOS = Next on Stack.
   - SP = Single-Precision Fixed Point
   - DP = Double-Precision Fixed Point
   - FP = Floating Point

2. All arithmetic operations and PWR place the result in NOS and then Pop the stack.

3. All derived functions except PWR place the result in TOS.

4. All derived FP functions destroy the contents of the stack. Only the result can be expected to be valid upon command completion.

5. Format conversion commands (FIXS, FIXD, FLTS, FLTD) require that FP data format be specified (command bits 5 and 6 must be 0).

6. NOS becomes TOS in POPS, POPD, POPF commands.

7. For the 7811B, one cycle = 488.9 nanoseconds.

8. All operation codes are hexadecimal values.
CHAPTER 2

INSTALLATION AND CHECKOUT

2.1 BOARD SETUP

If you are going to use CCSOFT, or will not use interrupts or on-board RAM/ROM, the 7811B is complete and ready to be plugged into your computer. No board setup is required and you may proceed to Section 2.2 below.

The 7811B has two jumper-selectable features. If you want the board to generate an Interrupt Request when the 9511A completes a command, solder a jumper into the INT jumper holes. If you are adding RAMs, solder a jumper into the RAM jumper holes. See Chapter 1, "Theory of Operation," for a fuller explanation of these jumper features.

If you decide to add the optional memory to the 7811B, carefully align the memory chips in the sockets (at the left of the board when the connector pins point toward you). Make sure that Pin 1 is in the upper left corner of the chip. Firmly seat the chip in the socket and check for curled or unseated pins. If everything looks fine, you are ready to install the board in your APPLE.
INSTALLATION AND CHECKOUT

2.2 INSTALLATION

WARNING: BEFORE REMOVING THE COMPUTER COVER, DISCONNECT THE POWER CORD FROM ITS SOCKET AT THE BACK OF THE COMPUTER. THIS WILL ELIMINATE THE POSSIBILITY OF ELECTRICAL SHOCK OR DAMAGE TO YOUR COMPUTER.

When the power cord has been disconnected, place the computer in front of you with the keyboard toward you. Place your hands palm-down on the back of the computer cover and curl your fingers around the back edge. Pull until you hear two distinct pops, then stop. Slide the cover to the rear until it is free of the computer and set it aside.

Toward the rear of your computer there are eight 50-pin connectors (usually colored green) with their slots aligned front-to-back. These are the peripheral connectors. They are numbered #0 through #7 from left to right. Slot #0 has special signals on some pins and is reserved for your CCS Model 7114 or other ROM card. The 7811B may reside in any other slot. We recommend that you use slot #1. If you use the CCSOFT ROM, the 7811B must reside in slot #1.

With the gold-plated connector pins pointing down and the component side of the board facing right, carefully align the connector contacts in the peripheral slot you choose. Gently but firmly push down on the card to seat it in the slot, making sure that you seat both the front and back ends of the connector tongue. Replace the computer cover, plug in the power cord, and you are ready to begin testing your new APU.
INSTALLATION AND CHECKOUT

2.3 CHECKOUT

When you turn the power on, watch for any sign of a problem, such as smoke or a funny sound. Such symptoms are rare, but the precaution is nonetheless important. You should hear the familiar beep and see the screen full of question marks. If anything else happens, IMMEDIATELY turn off the power. Disconnect the power cord, remove the computer cover, and make sure that all components are properly seated in their sockets and that the card is seated completely in its slot. Close up the computer and try the power on test again. If the problem persists, see your CCS Dealer.

The next test ensures that the 9511A is functioning. Although far from exhaustive, it tests the ability to enter commands and to read a floating point constant out of the stack. The command is: PUsh Pi onto the stack (PUP). The constant is the internal floating point representation of 3.1415926.

Test 1. Procedure:

a. Hit reset to initialize stack pointers
b. Enter "C091:1A(CR)"
c. Enter "C090.C097(CR)"
d. The display should show:

C090- 02 00 C9 00 0F 00 DA 00

Note that the first, third, fifth, and seventh bytes of step d. are the actual data bytes, while the second, fourth, sixth, and eighth bytes are the 9511A status bytes. This happens because the Command/Data port decoding of the 7811B only goes to the odd/even level within the 16 byte address block assigned to the peripheral connector. Step c. above sequentially accesses 8 of the 16 addresses, resulting in alternate data and status bytes being read and displayed.
CHAPTER 3

INTERFACE SOFTWARE

3.1 INSTALLATION OF CCSOFTWARE

To install the CCSOFTWARE software in your computer, insert the distribution diskette enclosed with your CCS 7811B Arithmetic Processor Unit into your disk drive and do a normal boot of the DOS. Then type in:

LOAD CCSOFTWAREn (cr)

where n is the number of the slot in which you have installed the 7811B APU module. Now remove the distribution diskette, insert your own initialized diskette, and type in:

SAVE APPLESOFT (CR)

To use CCSOFTWARE, merely type in:

FP (cr)

as you normally would. It runs the same as APPLESOFT II does.

Other programs on the diskette include:

BENCH -- A benchmark program

COSHGR -- A demonstration program which graphs a hyperbolic cosine in HIRES.
INTERFACE SOFTWARE

This program runs on either APPLESOFT or CCSOFT. To get a normal text display after running it, type in:

    TEXT (cr)

Try running it under both APPLESOFT and CCSOFT and note the difference in speed.

3.2 SPECIAL PROGRAMMING NOTES

The AMD 9511A Arithmetic Processing Unit was designed to interface to a different microprocessor than the APPLE's 6502. Additionally, the APPLE itself has a peculiar quirk which, if not compensated for, will cause considerable programming problems with many peripheral chips such as the 9511A. Both of these problems can be compensated for through software.

First, if the 9511A is busy when you attempt to transfer data or commands to it, it will issue a "Not Ready" signal to tell the computer to wait. If the computer is trying to write data to the 9511A, it will ignore this busy signal until after the write operation is complete. In other words, the computer just jams the data in even though the 9511A has indicated that it is not ready. The results are unpredictable.

The solution to this problem is to ensure that the 9511A is not busy BEFORE attempting a write operation. This may be accomplished by reading the 9511A's status and testing Bit 7 for the Busy indication. When Bit 7 is zero the write operation may be performed without harm.

Second, the Apple has a peculiar quirk in it when performing a write operation using indexed addressing: after performing the write operation, it immediately initiates a read cycle. Short of modifying your computer, there is no way to word this secondary read. Since the 9511A is a stack-oriented processor, this write-read operation first puts the data in and pushes the stack down by one byte (write), then pops the stack up by one byte (read). The net effect makes
the stack appear stationary. The only data appearing in the stack is the last written byte.

Two possible solutions exist for this problem. Either don't use indexed addressing, or do a write-push stack one word-read sequence. The first method is easiest to implement but limits your flexibility. Since it involves direct addressing, a different software driver must be written for each slot in which the APU might be installed. This method does improve execution speed. The second method loses speed, but allows for one software driver regardless of slot assignment. This latter method can be implemented with the following code:

```
STA $C080,x
LDA #PTOS
STA $C081,x
LDA $C080,x
```

where, on entry, A = the data to be written, x = 16 times the slot number, $C080 is the hexadecimal data port base address, $C081 is the hexadecimal command port base address, and PTOS is the 9511A single-precision Push Top Of Stack command.

Note that this problem affects only data write operations. Commands may be written without any need to further adjust the stack.

APPLESOFT II has a command which allows you to create your own assembly language subroutines. This command is the USR(X) function. The APU takes advantage of this to increase the repertoire of functions available to you. Before you can use the USR function, though, you must tell APPLESOFII where to find the routine. This is done by POKEing the address of the routine into locations 11 and 12 of memory. Then you can treat the USR(X) function as if it were any function. You need not rePOKE the addresses until you want a different function performed.

To POKE the address into memory, issue:

```
POKE 11, (ADDR - 256*INT (ADDR/256))
POKE 12, (INT (ADDR/256))
```
INTERFACE SOFTWARE

Use the following values for ADDR:

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>DISKETTE ADDRESS</th>
<th>ROM ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARCSIN(X)</td>
<td>9999</td>
<td>61208</td>
</tr>
<tr>
<td>ARCCOS(X)</td>
<td>9994</td>
<td>61204</td>
</tr>
<tr>
<td>LOG10(X)</td>
<td>9989</td>
<td>61198</td>
</tr>
<tr>
<td>PI</td>
<td>9875</td>
<td>61084</td>
</tr>
<tr>
<td>INVERSE(X)</td>
<td>9938</td>
<td>61147</td>
</tr>
<tr>
<td>SINH(X)</td>
<td>9959</td>
<td>61166</td>
</tr>
<tr>
<td>COSH(X)</td>
<td>9962</td>
<td>61169</td>
</tr>
<tr>
<td>TANH(X)</td>
<td>9906</td>
<td>61115</td>
</tr>
</tbody>
</table>

3.3 BENCHMARKS:

Using the CCSOFT software, each floating point function was timed over 5000 repetitions and compared with the APPLESOFT floating point equivalent. The following times were achieved:

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>OVERHEAD</th>
<th>CCSOFT</th>
<th>AS II</th>
</tr>
</thead>
<tbody>
<tr>
<td>MUL</td>
<td>11.4 sec</td>
<td>17.6 sec</td>
<td>22.3 sec</td>
</tr>
<tr>
<td>FDIV</td>
<td>11.4</td>
<td>17.6</td>
<td>27.3</td>
</tr>
<tr>
<td>EXP</td>
<td>13.8</td>
<td>25.4</td>
<td>130.6</td>
</tr>
<tr>
<td>SQR</td>
<td>13.8</td>
<td>17.1</td>
<td>248.9</td>
</tr>
<tr>
<td>RND</td>
<td>13.8</td>
<td>18.4</td>
<td>29.9</td>
</tr>
<tr>
<td>LOG</td>
<td>13.8</td>
<td>26.4</td>
<td>114.3</td>
</tr>
<tr>
<td>COS</td>
<td>13.8</td>
<td>26.6</td>
<td>135.2</td>
</tr>
<tr>
<td>PWR</td>
<td>11.4</td>
<td>41.1</td>
<td>153.9</td>
</tr>
<tr>
<td>TAN</td>
<td>13.8</td>
<td>28.7</td>
<td>244.8</td>
</tr>
<tr>
<td>ATN</td>
<td>13.8</td>
<td>29.2</td>
<td>222.4</td>
</tr>
<tr>
<td>INT</td>
<td>13.8</td>
<td>16.6</td>
<td>17.1</td>
</tr>
<tr>
<td>ACOS</td>
<td>13.8</td>
<td>30.6</td>
<td>554.8</td>
</tr>
<tr>
<td>ASIN</td>
<td>13.8</td>
<td>30.4</td>
<td>472.3</td>
</tr>
<tr>
<td>LOG(10)</td>
<td>13.8</td>
<td>26.8</td>
<td>325.6</td>
</tr>
<tr>
<td>PI</td>
<td>11.4</td>
<td>14.8</td>
<td>53.7</td>
</tr>
<tr>
<td>INV</td>
<td>11.4</td>
<td>16.6</td>
<td>29.6</td>
</tr>
<tr>
<td>SINH</td>
<td>13.8</td>
<td>37.7</td>
<td>266.5</td>
</tr>
<tr>
<td>COSH</td>
<td>13.8</td>
<td>37.4</td>
<td>265.4</td>
</tr>
<tr>
<td>TANH</td>
<td>13.8</td>
<td>62.0</td>
<td>403.1</td>
</tr>
</tbody>
</table>

Overhead is the time taken to execute the common code for both CCSOFT and APPLESOFT II. It was obtained using the following program:
INTERFACE SOFTWARE

10 B = 2: C = 3
20 FOR I = 1 TO 5000
30 A = B
40 NEXT
50 PRINT "DONE"

or the above program with line 30 changed to

30 A = ABS(I)

Line 30 was then altered to test each function and the program was run under both CCSOFT and APPLESOFT. For example, to test the square root function line 30 was altered to

30 A = SQR(I)

The significant speed advantage of the 7811B is readily apparent.
CHAPTER 4

TECHNICAL INFORMATION
### TECHNICAL INFORMATION

#### 4.2 PARTS LIST

**MODEL 7811B ARITHMETIC PROCESSOR UNIT**

**ASSY NO. 00000-7811B**

<table>
<thead>
<tr>
<th>#</th>
<th>QTY</th>
<th>REF</th>
<th>CCS P/N</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>C1-3,5</td>
<td>42034-21046</td>
<td>CAPACITOR, MONOLITHIC .1uf, 50vdc</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>C4</td>
<td>42215-52715</td>
<td>CAPACITOR, FIXED; MICA 270pf, 500vdc, 10%</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>Q1</td>
<td>36100-02907</td>
<td>TRANSISTOR, SI; PNP GENERAL PURPOSE, PN2907</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>R1-5</td>
<td>40002-02215</td>
<td>RESISTOR, FIXED, COMP 220 ohm, 1/4W, 10%</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>R6</td>
<td>40002-02725</td>
<td>RESISTOR, FIXED, COMP 2.7K ohm, 1/4W, 10%</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>U1</td>
<td>31900-09511</td>
<td>IC, DIGITAL, MOS; AM9511 ARITHMETIC PROCESSOR</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>U2</td>
<td>30000-00000</td>
<td>IC, DIGITAL, TTL; 74LS00 QUAD 2 IN NAND</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>U3</td>
<td>30000-00074</td>
<td>IC, DIGITAL, TTL; 74LS74 DUAL D FLIP FLOP</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>U6</td>
<td>30900-08304</td>
<td>IC, DIGITAL, TTL; 8304B OCTAL BUS DRV/R CVR</td>
</tr>
<tr>
<td>10</td>
<td>2</td>
<td>U7</td>
<td>30000-00004</td>
<td>IC, DIGITAL, TTL; 74LS04 HEX INVERTER</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>U8</td>
<td>30000-00009</td>
<td>IC, DIGITAL, TTL; 74LS09 QUAD 2 IN AND (OC)</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>U9</td>
<td>30000-00003</td>
<td>IC, DIGITAL, TTL; 74LS03 QUAD 2 IN NAND (OC)</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>Z1</td>
<td>40930-72726</td>
<td>RESISTOR NETWORK, SIP 2.7K x 7</td>
</tr>
<tr>
<td>14</td>
<td>5</td>
<td>XU2,3,9</td>
<td>58102-00140</td>
<td>SOCKET, IC; LOW PROFILE 14 PIN DIP</td>
</tr>
<tr>
<td>15</td>
<td>2</td>
<td>XU4,5</td>
<td>58102-00160</td>
<td>SOCKET, IC; LOW PROFILE 16 PIN DIP</td>
</tr>
<tr>
<td>16</td>
<td>1</td>
<td>XU6</td>
<td>58102-00200</td>
<td>SOCKET, IC; LOW PROFILE 20 PIN DIP</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>XU1</td>
<td>58102-00240</td>
<td>SOCKET, IC; LOW PROFILE 24 PIN DIP</td>
</tr>
<tr>
<td>18</td>
<td>1</td>
<td>-</td>
<td>07811-00002</td>
<td>BOARD, PC APU-1, REV B</td>
</tr>
<tr>
<td>19</td>
<td>-</td>
<td>A/R</td>
<td>51000-01220</td>
<td>WIRE, BARE; TINNED #22 AWG</td>
</tr>
</tbody>
</table>

4-3
4.3 ASSEMBLY COMPONENT BREAKDOWN

ALL NUMBERS REFERENCE PARTS LIST
4.4 APPLE II I/O CONNECTOR CONFIGURATION

TOP VIEW

GND 26
DMA IN 27
INT IN 28
NM 29
IRQ 30
RES 31
INH 32
-12V 33
-5V 34
N.C. 35
7M 36
Q3 37
Φ1 38
USER 1 39
Φ0 40

DEVICE SELECT 41
D7 42
D6 43
D5 44
D4 45
D3 46
D2 47
D1 48
D0 49
+12V 50

BACK OF APPLE MAIN BOARD

25 +5V
24 DMA OUT
23 INT OUT
22 DMA
21 RDY
20 I/O STROBE
19 N.C.
18 R/W
17 A15
16 A14
15 A13
14 A12
13 A11
12 A10
11 A9
10 A8
9 A7
8 A6
7 A5
6 A4
5 A3
4 A2
3 A1
2 A0
1 I/O SELECT

FRONT OF APPLE MAIN BOARD
TECHNICAL INFORMATION

4.5  7811B BOARD DIMENSIONS

Measurements in inches
APPENDIX A

THE CCSOFT ROM

A.1 INTRODUCTION

The addition of the CCS 7811B to your system significantly increases the power of your APPLE II. The CCSOFT ROM makes the fast floating-point arithmetic capabilities of the CCS 7811B available to users of the APPLESOFT ROM Card and APPLE II+. Now you can unleash the computational speed of the 7811B upon both pages of high-resolution graphics, increase the functions available to you through easy-to-use USR(x) functions, and speed up most other computational tasks.

This chip may be installed in any of three different ways, depending upon your circumstances and, to some degree, your desires. First, if you have an APPLESOFT Firmware Card, this chip directly replaces one of the ROMs on that card. Second, if you have an APPLE II+, this ROM will directly replace one of the ROMs on the main board of your computer. Last, if you have an APPLE II+ and wish to be able to switch (under software control) between the slightly increased accuracy of the normal APPLESOFT arithmetic and the speed of the 7811B arithmetic, then this ROM may be mounted on a CCS 7114 PROM/ROM Board. In all three cases the 7811B APU must reside in slot #1.
A.2 INSTALLATION AND CHECKOUT

A.2.1 APPLESOFT ROM Card:

a. Place your APPLESOFT ROM Card in front of you with the switch to the right.

b. Just above the top row of chips the numbers 1 to 8 are printed. Carefully remove the chip immediately below the number 4.

c. Orient the CCSoft ROM chip over the number 4 socket so that Pin 1 is toward the top of the board. The Pin 1 mark will be some sort of notch at the end of the chip or a dot or number in the corner next to Pin 1. If you hold the chip so the writing is right-side-up, Pin 1 should be in the lower left-hand corner.

d. Set the chip down onto the socket, carefully aligning the pins into the socket holes.

e. Firmly but gently seat the chip into the socket.

f. Inspect the chip seating. If any pins are unseated or curled under, carefully remove and reseat the chip.

g. Install the card in your computer as you normally would.

h. Make sure that the CCS 7811B Arithmetic Processor Unit is installed in Slot #1.

i. Close your computer and you are on your way.
THE CCSOFT ROM

A.2.2 APPLE II+:

a. Place your computer in front of you.

b. UNPLUG THE POWER CORD FROM ITS SOCKET AT THE REAR OF YOUR COMPUTER. FAILURE TO DO SO COULD CAUSE ELECTRICAL SHOCK AND/OR DAMAGE TO YOUR COMPUTER.

c. Remove the top cover according to the instructions in your APPLE Reference Manual.

d. About 6 inches from the rear of the computer is a row of 6 larger chips. On the circuit board just in front of the chips are silk-screened circuit designators for the chips. Locate the chip designated ROM-E8.

e. Remove the chip. The ROM itself will be marked 341-0014-00. Place it aside.

f. Orient the CCSOFT ROM over the now-empty socket with Pin 1 toward you. (See II.1.c above for Pin 1 mark identification.)

g. Carefully align the CCSOFT ROM pins into the socket.

h. Firmly but gently seat the chip into the socket.

i. Inspect the chip seating. If any pins are unseated or curled under, carefully remove and reseat the chip.

j. Make sure that your CCS 7811B Arithmetic Processor Unit is installed in Slot #1.

k. Replace the cover on your computer and you are on your way.
THE CCSOFT ROM

A.2.3 APPLE II+ with CCS 7114 PROM/ROM Card:

a. Place the 7114 PROM/ROM board in front of you with the switch to the right.

b. Observing the Pin 1 mark, align the CCSOFT ROM into the socket labeled E8. (See II.1.c. above for Pin 1 mark identification.)

c. Firmly but gently seat the ROM into the socket.

d. Inspect the ROM seating. If any pins are unseated or curled under, carefully remove and reseat the ROM.

e. Install a 1N4148 or 1N914 diode into the D10 position on the lower left of the board. Be sure to take into account the diode's polarity.

f. Install the 7114 PROM/ROM Card into Slot #0.

g. Make sure the 7811B Arithmetic Processor Unit is in Slot #1.

h. Close up your computer and you are on your way.

A.2.4 Checkout

Testing whether CCSOFT is working is a simple matter. Type in:

?SQR(2)(CR)

Because CCSOFT truncates instead of rounds, it will give a slightly different answer than APPLESOFT. If the result is 1.41421354, CCSOFT is working. If the last digit is a 6 rather than a 4, APPLESOFT is working and something is wrong. Go over the installation procedures to make sure the ROM is properly installed. If improper installation is not the problem, see your dealer.
APPENDIX B

LIMITED WARRANTY

California Computer Systems (CCS) warrants to the original purchaser of its products that

1.) its CCS assembled and tested products will be free from materials defects for a period of one (1) year, and be free from defects of workmanship for a period of ninety (90) days; and

2.) its kit products will be free from materials defects for a period of ninety (90) days.

The responsibility of CCS hereunder, and the sole and exclusive remedy of the original purchaser for a breach of any warranty hereunder, is limited to the correction or replacement by CCS at CCS's option, at CCS's service facility, of any product or part which has been returned to CCS and in which there is a defect covered by this warranty; provided, however, that in the case of CCS assembled and tested products, CCS will correct any defect in materials and workmanship free of charge if the product is returned to CCS within ninety (90) days of original purchase from CCS; and CCS will correct defects in materials in its products and restore the product to an operational status for a labor charge of $25.00, provided that the product is returned to CCS within ninety (90) days in the case of kit products, or one (1) year in the case of CCS assembled and tested products. All such returned products shall be shipped prepaid and insured by original purchaser to:

B-1
LIMITED WARRANTY

Warranty Service Department
California Computer Systems
250 Caribbean Drive
Sunnyvale, California
94086

CCS shall have the right of final determination as to the existence and cause of a defect, and CCS shall have the sole right to decide whether the product should be repaired or replaced.

This warranty shall not apply to any product or any part thereof which has been subject to

(1) accident, neglect, negligence, abuse or misuse;
(2) any maintenance, overhaul, installation, storage, operation, or use, which is improper; or
(3) any alteration, modification, or repair by anyone other than CCS or its authorized representative.

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CCS's obligations under this warranty are conditioned on the original purchaser's maintenance of explicit records which will accurately reflect operating conditions and maintenance performed on CCS's products and establish the nature of any unsatisfactory condition of CCS's products. CCS, at its request, shall be given access to such records for substantiating warranty claims. No action may be brought for breach of any express or implied warranty after one (1) year from the expiration of this express warranty's applicable warranty period. CCS assumes no liability for any events which may arise from the use of technical information on the application of its products supplied by CCS. CCS makes no warranty whatsoever in respect to accessories or parts not supplied by CCS, or to the extent that any defect is attributable to any part not supplied by CCS.

CCS neither assumes nor authorizes any person other than a duly authorized officer or representative to assume for CCS any other liability or extension or alteration of this warranty in connection with the sale or any shipment of CCS's products. Any such assumption of liability or modification of warranty must be in writing and signed by such duly authorized officer or representative to be enforceable. These warranties apply to the original purchaser only, and do not run to successors, assigns, or subsequent purchasers or owners; AS TO ALL PERSONS OR ENTITIES OTHER THAN THE ORIGINAL PURCHASER, CCS MAKES NO WARRANTIES WHATSOEVER, EXPRESS OR IMPLIED OR STATUTORY. The term "original purchaser", as used in this warranty shall be deemed to mean only that person to whom its product is originally sold by CCS.

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