

### 3.3 DC Characteristics of Interface Signals

#### 3.3.1 Output Drive

<u>Name</u>	<u>Output Current</u> (milliamps)		<u>Output Voltage</u> (volts)	
	<u>IOH</u>	<u>IOL</u>	<u>VOH</u>	<u>VOL</u>
RD*	-1.0	6.5	2.4	0.5

#### 3.3.2 Input Loading

<u>Name</u>	<u>Input Current</u> (milliamps)		<u>Input Voltage threshold</u> (volts)	
	<u>VIH=2.4V</u> <u>IIH</u>	<u>VIL=0.4V</u> <u>IIL</u>	<u>VIH</u>	<u>VIL</u>
WRDATA*, /WRTGATE*	-0.9	-1.5	2.0	0.8
CA0-CA2, LSTRB, SEL	0.1	-0.25	2.0	0.8
/ENBL	0.125	-0.75	2.2	0.8
/PWM	0.01	-0.04	2.0	0.8

\*These signal lines include a 3.3K pull-up resistor to +5v.

#### 3.4 Timing Requirements

The following sections contain timing diagrams which show the relationship between the input and output signals.

 **apple computer inc.**

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699-0285-A

SCALE:

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