3.3 DC Characteristics of Interface Signals

3.3.1 Output Drive
3.3.2 Input Loading

3.4 Timing Requirements

3.4.1 Reading one of the Status Signals
3.4.2 Sending one of the Control Commands
3.4.3 /WRTGATE, WRTDATA and /ERASE Timing
3.4.4 /DIRTN and /STEP Timing
3.4.5 /TK0 Timing
3.4.6 RDDATA Valid Timing (1)
3.4.7 RDDATA Valid Timing (2)
3.4.8 /PWM Waveform

3.5 Power On and Power Off Requirements

3.5.1 Data Protection
3.5.2 Power Supply Sequencing
3.5.3 Head Position Initialization at Power On

3.6 Interface Connector and Pin Assignment

4.0 Labelling

4.1 Label Position

4.2 Label Contents

Appendix A. Jitter Generator Schematic

Appendix B. Format Description