ENSONIQ D0C ERS

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Rev. 1.0

ENSONIQ GENERAL DESCRIPTION

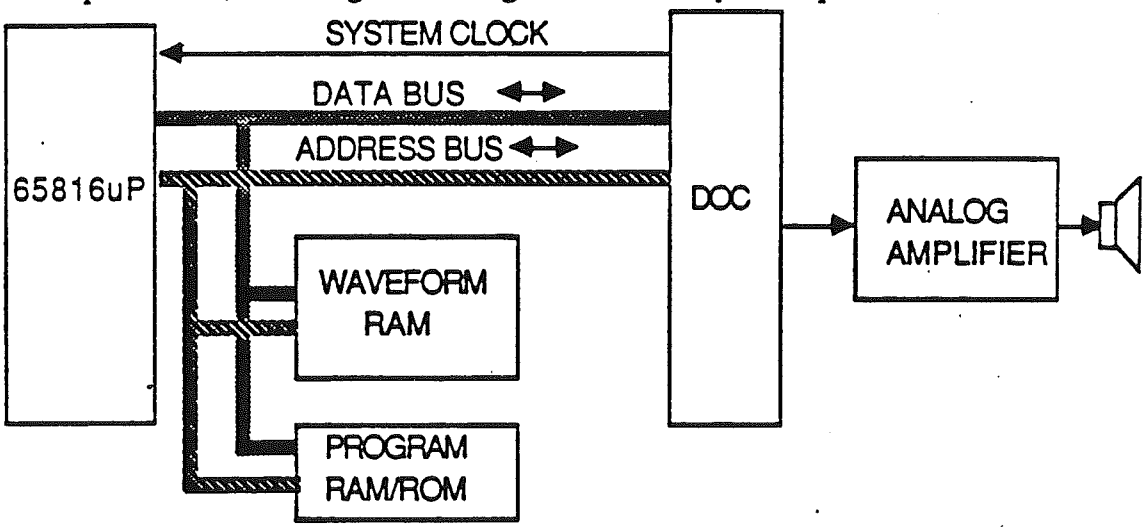
The 5503 Digital Oscillator Chip (DOC) provides high quality music synthesis capabilities for sound related applications. These applications range from arcade and home video games to a professional music synthesizers. The 5503 contains 32 digital sampling oscillators, various control registers and an eight bit analog to digital converter.

FEATURES

- Powerful sound capabilities with low processor intervention.
- Directly addresses 64k bytes of memory
- Bank swapping allows for an additional 64k bytes of memory
- Up to 16 channel voice assignment
- Easy to interface to dynamic memory

OPERATIONS DESCRIPTION

This is a digital sampling oscillator chip that has been designed by Ensoniq for use in their professional synthesizers products. Sound are produced from digitized waveforms stored in ram called wavetables. The DOC is designed to work with a 65815 style microprocessor, taking advantage of the way the processor works.

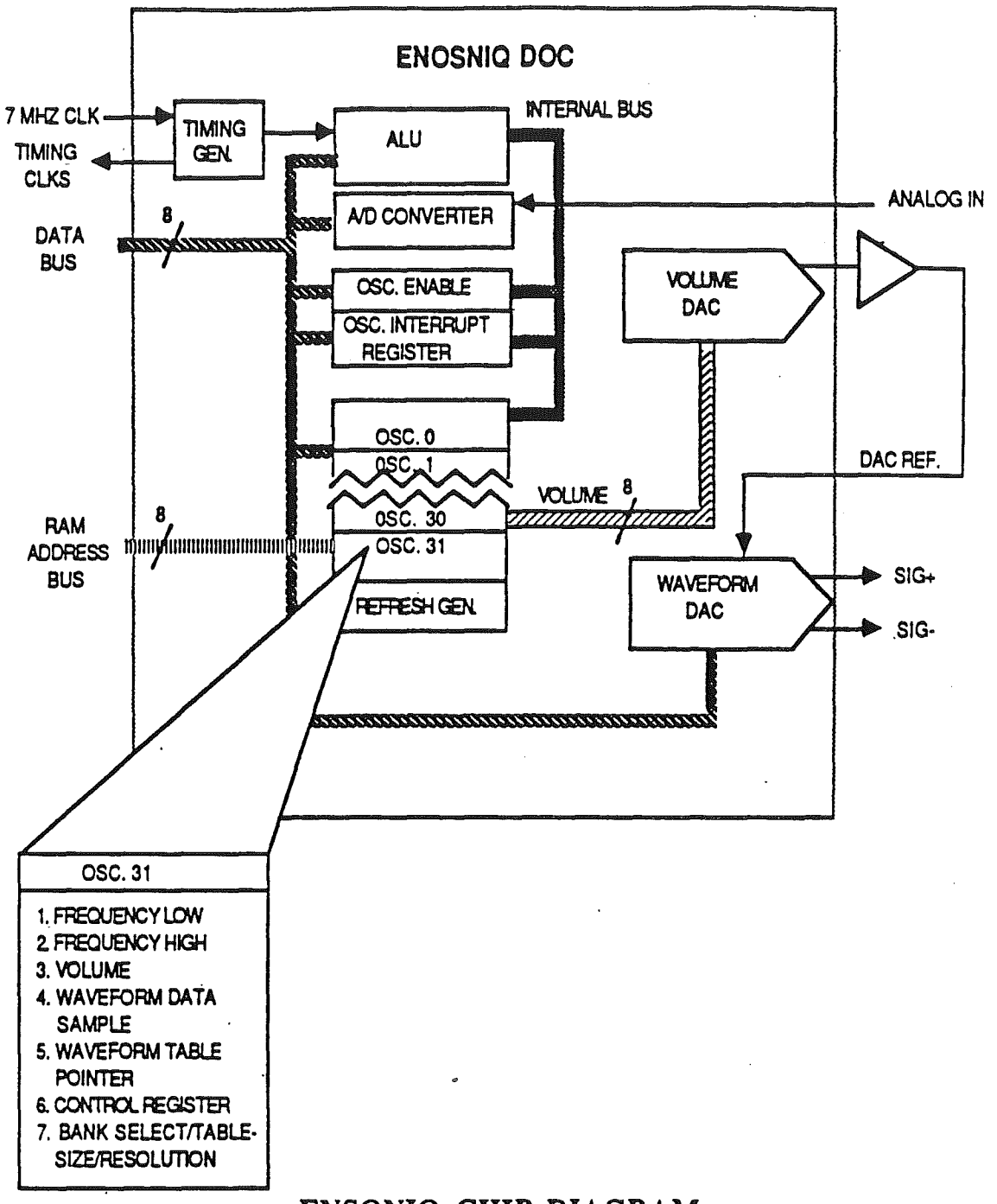


SIMPLIFIED SYSTEM BLOCK DIAGRAM

The DOC contains 32 time multiplexed digital oscillators to generate addresses that increment through the wavetable. The microprocessor and DOC share access to the data and address bus on alternating phases of a symmetrical system clock. While the clock is high the processor takes control, performing a read or write from

ram or the DOC, on the other phase the processor performs internal operations and the DOC takes over. During each DOC cycle, an oscillator sends out an address to read a byte from its wavetable stored in ram. The data that is read from the wavetable is sent to the output section of the DOC consisting of two cascaded eight bit Digital to Analog Converters (DACs) where the waveform is turned into audio. The upper DAC contains the volume and the lower DAC contains the waveform information. Each oscillator gets a cycle until all of the oscillators have updated there waveform, then the next two cycles are used for refreshing dynamic rams and the process starts over again. Even though during one scan of all the oscillators and each oscillator has only output a step of its total waveform the results are integrated over time to create the sounds of many different pitches and timbers.

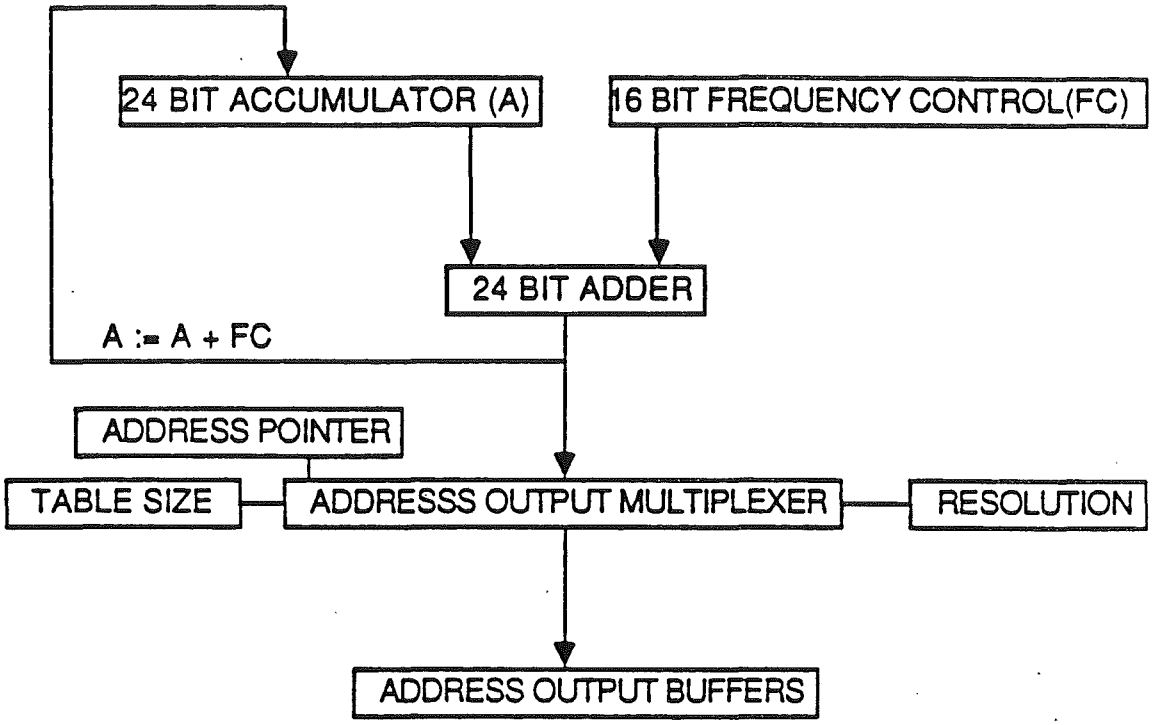
There are 7 registers per oscillator to control the frequency rate at which an oscillator steps through its wavetable, the size, and starting address in memory, and the mode in which it oscillates. In addition to these 224 register, there are 3 additional register for interrupts, enabling oscillators and an 8 bit analog to digital converter.



ENSONIQ CHIP DIAGRAM

OSCILLATORS

Oscillators are actually address generators. They step through a waveform table at a rate that is determined by the frequency control register and the resolution register.



OSCILLATOR BLOCK DIAGRAM

Each time an oscillator is updated the value that is stored in the frequency control register is added with the 24 bit accumulator by a 24 bit adder . This new value is stored back into the accumulator and is also passed to the address multiplexer to form the final 16 bit ram address. In the address multiplexer the resolution register will determine which 16 bits of the accumulator that can be used for the the final address. The table size register is used to determine how many of the available 16 bits of accumulator that will form the final address. The pointer register sets the remaining most significant bit(s) in the final address. The number of pointer bits used is determined by the table size register this will be explained in more detail later.

REGISTER DESCRIPTION

FREQUENCY CONTROL LOW AND HIGH ($00-$1F, $20-$3F) This group of registers form, in part the actual frequency in which the DOC steps through the waveform table. The FREQUENCY LOW and the FREQUENCY HIGH registers are concatenated to form a 16-bit incremental value for the 24 bit linear accumulator. Each time the oscillator is updated the value of the high/low FREQUENCY CONTROL REGISTER is added to the current value stored in the accumulator. The following equations can be used to determine the final output frequency.

- SR = CLK / ((OSC + 2) * 8)

  Fundamental Output Frequency. = [SR / $2^{(17 + RES)}$] * FC

  Where: SR = sample rate, CLK = input clock, OSC = enabled oscillators, RES = Resolution register, FC is the Frequency high and Frequency Low registers concatenated, and the waveform fundamental frequency length is equal to one page of memory.

VOLUME ($40-$5F) This set of registers is used to control the volume level of the waveform data. The current value read by the associated oscillator from the waveform table is multiplied by the eight bit volume register to obtain the final output level for the oscillator. It should be noted that volume register is ignored when the associated oscillator is running in self enveloping mode.

DATA SAMPLE ($60-$7F) This set of read only registers contain last value read from the waveform table for the corresponding oscillator.

ADDRESS POINTER ($80-$9F) This set of registers contain the beginning page number of the waveform table address and are used to determine the final ram address. All waveform tables must begin at the first address of a page. Also, a waveform table cannot wrap around from upper to lower memory. For example, an 8k table cannot start at the highest page of memory and continue through lower memory. Therefore, the larger the table size, the fewer of the pointer bits are actually used. The follow table indicates how each bit affects the address offset:

TABLE SIZE	POINTER BITS USED							
256	P7	P6	P5	P4	P3	P2	P1	P0
512	P7	P6	P5	P4	P3	P2	P1	X
1024	P7	P6	P5	P4	P3	P2	X	X
2048	P7	P6	P5	P4	P3	X	X	X
4096	P7	P6	P5	P4	X	X	X	X
8192	P7	P6	P5	X	X	X	X	X
16384	P7	P6	X	X	X	X	X	X
32768	P7	X	X	X	X	X	X	X

X = ignored

CONTROL REGISTER ($A0-$BF)

The control register determines the channel assignment, oscillator mode, and the Halt bit. The following is the control register bit positions:

D7	D6	D5	D4	D3	D2	D1	D0
CA3	CA2	CA1	CA0	IE	M1	M0	H

CA0-CA3 (Channel Assignment) These bits are used to control an external analog multiplexer. This is would then route each oscillator to a particular channel. A typical synthesizer would have eight channels with four oscillators assigned to a channel or "voice," as it is commonly called. Each voice would then have a programmable filter to control the harmonic content of the waveform as time progresses. This reduces the amount of data needed to synthesize an instrument.

IE (Interrupt Enable) When this bit is set to a one, interrupts will be passed to the Oscillator Interrupt Register (OIR) when an oscillator completes its cycle. If more than one oscillator has generated an interrupt, the consecutive interrupts will be put on the interrupt stack to be processed in a first in first out order. If the IE bit is a zero, then when the oscillator completes it cycle the oscillator status will be passed to the an interrupt table, but will not be passed to the OIR. However if the IE bit is changed to a one then the interrupt will be sent to the OIR.

M0-M1 (MODE) These two bits are used to set the oscillating mode of each oscillator.

M1	M0	OSCILLATOR FUNCTION
0	0	Free Run Mode
0	1	One-Shot Mode
1	0	Sync/AM Mode
1	1	Swap Mode

Free Run Mode - In this mode the oscillator runs in a continuous loop, repeating the same waveform until it is halted by the controlling microprocessor, or encounters a zero in the waveform table.

One-Shot Mode - In this mode the oscillator cycles through the waveform table once, halting at the end of the table.

Sync/AM Mode This mode uses pairs of adjacent-numbered oscillators and depending on whether the lower oscillator is odd or even determines the mode. To select AM mode use an odd/even pair, to select sync mode use an even/odd pair.

AM Mode - In this mode, the odd oscillator is used to amplitude modulate the even oscillator. When in this mode, the volume register is ignored for the pair of registers. This mode also requires the analog waveform to be gated with CSTRB.

Sync Mode - When in this mode the higher odd oscillator will sync on to the lower even oscillator. When the first oscillator wraps around to the beginning of its table, the second oscillator is also reset to the beginning of its table.

Swap Mode - This mode uses pairs of oscillators where the lower oscillator is even, the higher is odd. The oscillator runs in a one-shot mode, when it completes its cycle it resets its accumulator to zero and clears the halt bit of the next oscillator.

H (Halt Bit) This bit indicates when an oscillator has been halted by either the DOC or the micro-processor. When M0 = 1 * H = 1, the oscillators accumulator will be reset to zero. An oscillator will halt when a zero is encountered in its waveform table. Because some memory locations maybe skipped do to the frequency the oscillator is set to, eight consecutive zeros must be in memory to guarantee the oscillator will halt.

WAVEFORM TABLE SIZE/RESOLUTION/BANK SELECT ($C0-$DF)

This group of registers is used to control three oscillator functions. The following chart indicates the bit positions within the register:

D7	D6	D5	D4	D3	D2	D1	D0
X	BS	T2	T1	T0	R2	R1	R0

BS- (Bank Select) This bit is used to extend the addressing range of the DOC. If BS = 0 then the DOC address range is 0 to 64k, if BS = 1 then the DOC address range is 65k to 128k.

T2-T0 (Table size) These bits are used to specify the size of the waveform table addressed by the oscillator and are used to determine the final ram address. The maximum addressable memory for an oscillator is 32k. The following table indicates there usage:

T2	T1	T0	Table Size in bytes
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

R2-R0 (Resolution) These bits determine which16 of the 24-bits of the oscillator accumulator used to determine the final address into the waveform table. Typically the Resolution register would be loaded with the same value that is in the Table Size register otherwise the Resolution register affects the fundamental frequency by powers of 2.

R2	R1	R0	Accumulator bits
0	0	0	1 through 16
0	0	1	2 through 17
0	1	0	3 through 18
0	1	1	4 through 19
1	0	0	5 through 20
1	0	1	6 through 21
1	1	0	7 through 22
1	1	1	8 through 23

OSCILLATOR INTERRUPT REGISTER ($E0)
The Oscillator Interrupt Register (OIR) contains the state of the IRQ line and the number of an interrupting oscillator, if any. When an oscillator completes a waveform table and the EI bit is set to a one, the number of the oscillator will be passed to the OIR. The OIR will force the IRQ line low indicating an interrupt, bit 7 will be set to a zero, and bits 5-1 will contain the number of the interrupting oscillator. The following is the bit position of the OIR:

D7	D6	D5	D4	D3	D2	D1	D0
IRQ	1	O4	O3	O2	01	O0	1

If more than one oscillator is generating an interrupt, unprocessed interrupts will be put into a interrupt stack. After the processor reads the OIR, the DOC will clear the appropriate interrupt request and the next pending interrupt, if any, will be pulled off of the interrupt stack and put in the OIR. Note that bits 0 and 6 are always read back as 1's.

OSCILLATOR ENABLE ($E1) This register controls the number of active oscillators in the DOC. A minimum of one oscillator is always selected, which is also the reset default. To enable oscillators multiply the desired number by 2, i.e. to enable all 32 oscillators load the register with 64.

A/D CONVERTER ($E2) This register contains the value of the A/D converter. A read from this register initiates the A to D conversion. Conversion time is 26 cycles. If the A/D register is read before the conversion is complete, the value will be lost and a new conversion will start.

REGISTER SUMMARY

ADDRESS	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
$00-$1F	FREQUENCY LOW	FL7	FL6	FL5	FL4	FL3	FL2	FL1	FL0
$20-$3F	FREQUENCY HIGH	FH7	FH6	FH5	FH4	FH3	FH2	FH1	FH0
$40-$5F	VOLUME	V7	V6	V5	V4	V3	V2	V1	V0
$60-$7F	WAVEFORM DATA SAMPLE	W7	W6	W5	W4	W3	W2	W1	W0
$80-$9F	WAVEFORM TABLE POINTER	P7	P6	P5	P4	P3	P2	P1	P0
$A0-$BF	CONTROL	CA3	CA2	CA1	CA0	IE	M1	M0	H
$C0-$DF	BANK SELECT/ TABLE SIZE/ RESOLUTION	X	BS	T2	T1	T0	R2	R1	R0
$E0	OSCILLATOR INTERRUPT	IRQ	X	O4	O3	O2	01	O0	X
$E1	OSCILLATOR ENABLE	X	X	E4	E3	E2	E1	E0	X
$E2	A/D CONVERTER	A7	A6	A5	A4	A3	A2	A1	A0

NOTE: Bits labeled as X's are not used and always read back as a 1.

FINAL ADDRESS CALCULATION

The final address can be calculated using the following table.

TABLE SIZE	FINAL ADDRESS																RESOLUTION		
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R2	R1	R0
256	POINTER REGISTER P7 ◄——► P0								A23 ◄——► A16 ACCUMULATOR BITS A16 ▼ A9								1 ▼ 0	1 ▼ 0	1 ▼ 0
512	P7						P1	A23 ▼ A16								A15 ▼ A8	1 ▼ 0	1 ▼ 0	1 ▼ 0
1024	P7					P2	A23 ▼ A16									A14 ▼ A7	1 0	1 0	1 0
2048	P7				P3	A23 ▼ A16										A13 ▼ A6	1 0	1 0	1 0
4096	P7			P4	A23 ▼ A16											A12 ▼ A5	1 0	1 0	1 0
8192	P7		P5	A23 ▼ A16												A11 ▼ A4	1 0	1 0	1 0
16384	P7	P6	A23 ▼ A16													A10 ▼ A3	1 0	1 0	1 0
32768	P7	A23 ▼ A16														A9 ▼ A2	1 0	1 0	1 0

For example, a waveform that is 512 bytes long, and the resolution register is set for 7, then pointer bits 1 through 7 and accumulator bits 15 through 23 will make up the final address. If the resolution register were now changed to 5, then pointer bits 1 through 7 and accumulator bits 12 through 21 would make up the final address.