Z85C30

CMOS SCC SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Serial Communications Controller, Z85C30 SCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's non-multiplexed address/ data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10x19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported as is standard for Zilog peripheral components.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

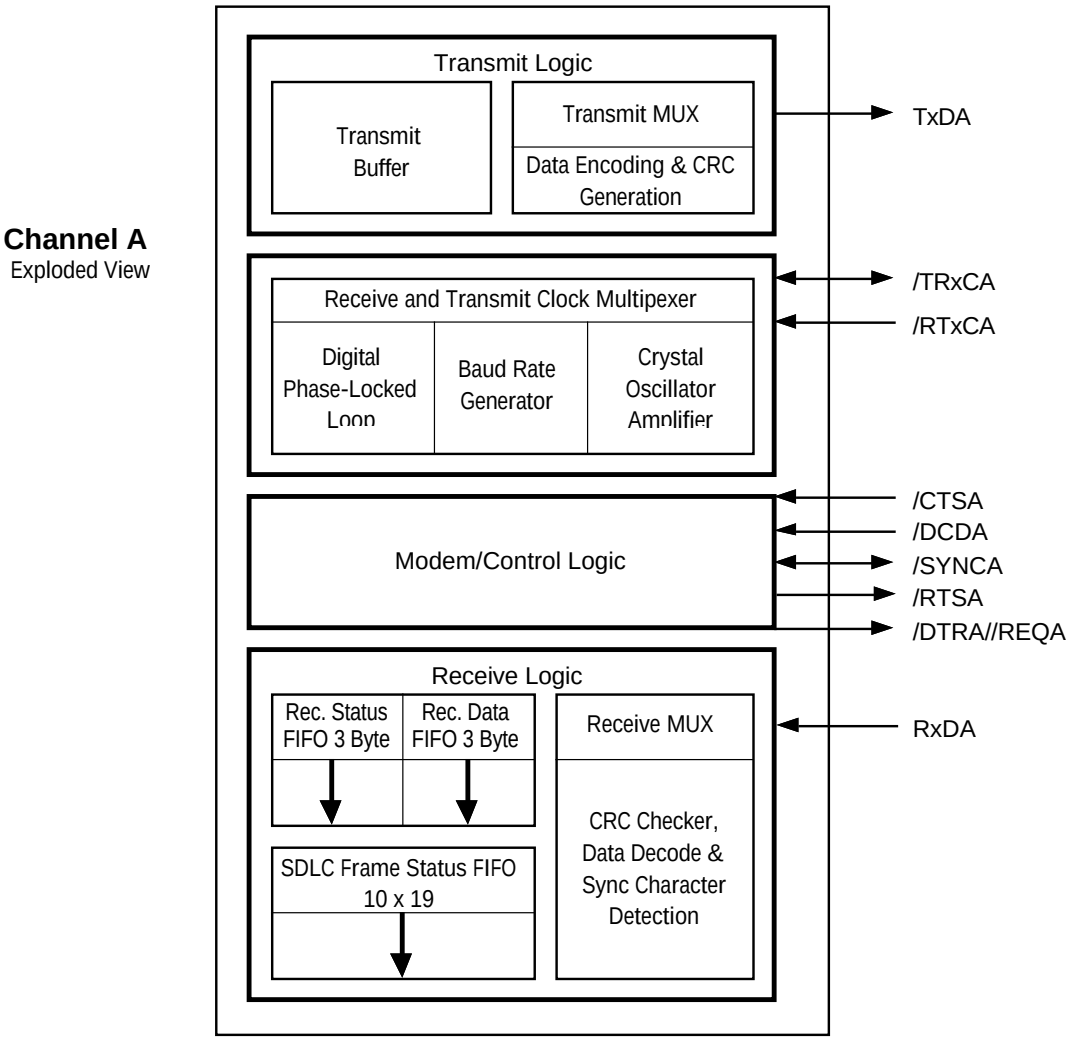
Power connections follow conventional descriptions below:

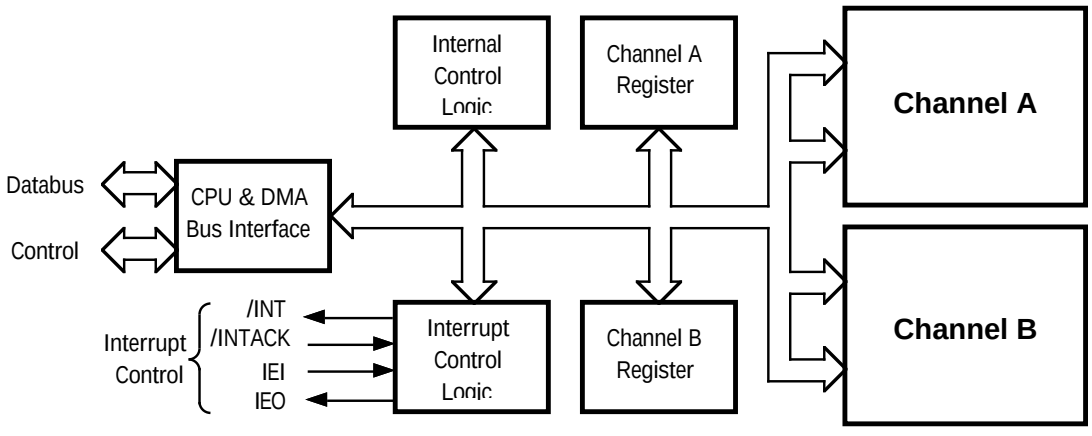
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

The description on Z85C30 is applicable to the following parts:

Z85C3008PSC
Z85C3010PSC
Z85C3016PSC
Z85C3008VSC
Z85C3010VSC
Z85C3016VSC

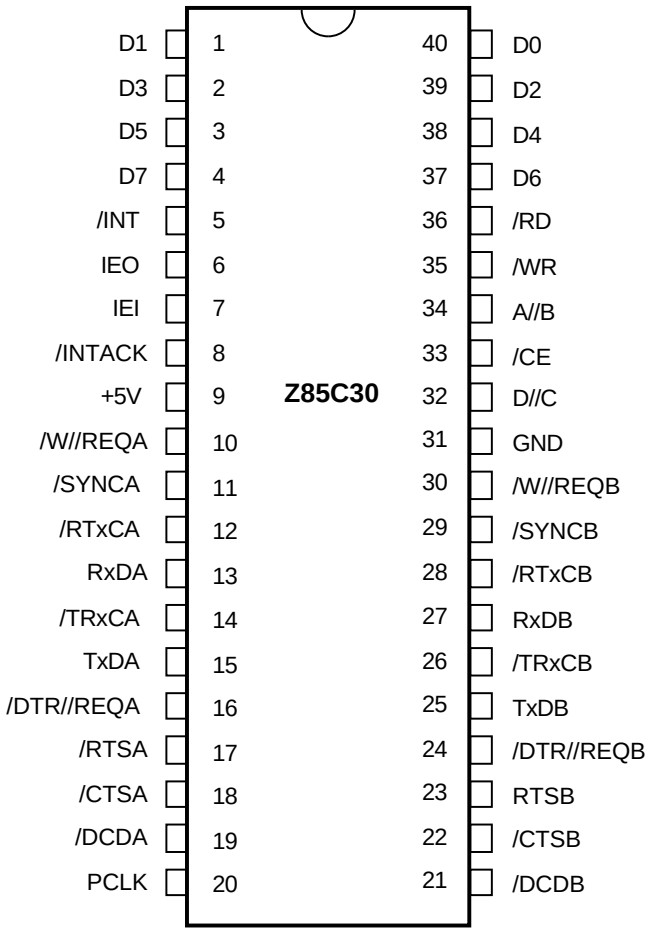
GENERAL DESCRIPTION (Continued)



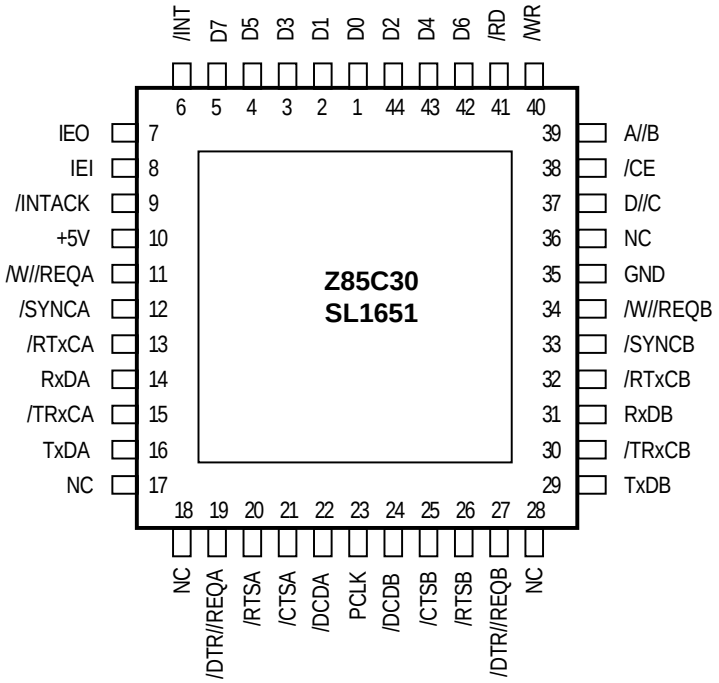


SCC Block Diagram

PIN ASSIGNMENTS



Z85C30
DIP Pin Assignments



Z85C30
PLCC Pin Assignments

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:

* Voltage on all pins with respect to GND.
† See Ordering Information.

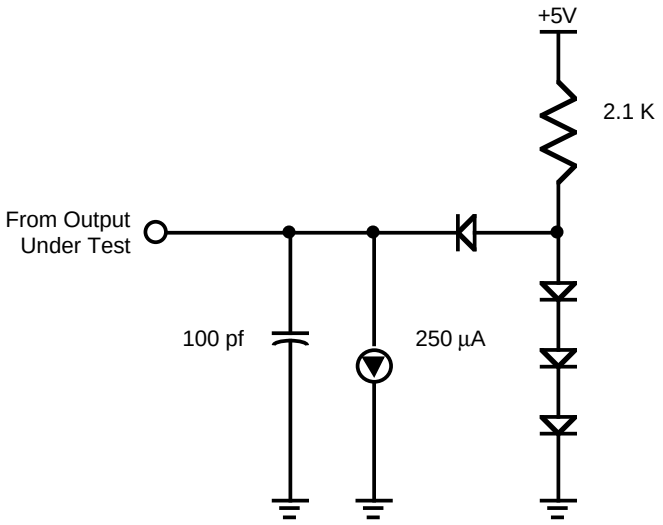
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

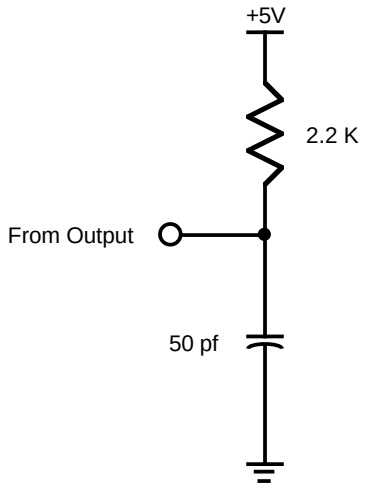
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- +4.50 V ≤ V_{CC} ≤ + 5.50 V
- GND = 0 V
- T_A as specified in Ordering Information



Standard Test Load



Open-Drain Test Load

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured pins
C_{OUT}	Output Capacitance		15	pF	returned to ground.
$C_{I/O}$	Bidirectional Capacitance		20	pF	

Note:
f = 1 MHz, over specified temperature range.

MISCELLANEOUS

Gate Count - 6800

DC CHARACTERISTICS

Z85C30

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = -1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8			V	I_{OH} = -250µA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = +2.0mA
I_{IL}	Input Leakage			±10.0	µA	0.4 <V_{IN} <+2.4V
I_{OL}	Output Leakage			±10.0	µA	0.4 <V_{OUT}<+2.4V
I_{CC1}	V_{CC} Supply Current		4	10 (8.5 MHz)	mA	
			5	12 (10 MHz)	mA	V_{CC}=5V V_{IH}=4.8 V_{IL}=0.2V
			7	15 (16 MHz)	mA	Crystal Oscillators off
			9	20 (20 MHz)	mA	
I_{CCOSC}	Crystal OSC Current		6		mA	Current for each osc. in addition to I_{CC1}

Notes:

[1] V_{CC} = 5V ±10% unless otherwise specified, over specified temperature range.

[2] Typical I_{CC} was measured with oscillator off.

[3] No I_{CC}(osc) max is specified due to dependency on the external circuit.

AC CHARACTERISTICS

Z85C30 Read and Write Timing Table

			8.5 MHz		10 MHz		16 MHz	
No	Symbol	Parameter	Min	Max	Min	Max	Min	Max
1	TwPCl	PCLK Low Width	45	2000	40	2000	26	2000
2	TwPCh	PCLK High Width	45	2000	40	2000	26	2000
3	TfPC	PCLK Fall Time		10		10		5
4	TrPC	PCLK Rise Time		10		10		5
5	TcPC	PCLK Cycle Time	118	4000	100	4000	61	4000
6	TsA(WR)	Address to /WR Fall Setup Time	66		50		35	
7	ThA(WR)	Address to /WR Rise Hold Time	0		0		0	
8	TsA(RD)	Address to /RD Fall Setup Time	66		50		35	
9	ThA(RD)	Address to /RD Rise Hold Time	0		0		0	
10	TsIA(PC)	/INTACK to PCLK Rise Setup Time	20		20		15	

No	Symbol	Parameter	8.5 MHz Min	8.5 MHz Max	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes
11	TsIAi(WR)	/INTACK to /WR Fall Setup Time	140		120		70		[1]
12	ThIA(WR)	/INTACK to /WR Rise Hold Time	0		0		0		
13	TsIAi(RD)	/INTACK to /RD Fall Setup Time	140		120		70		[1]
14	ThIA(RD)	/INTACK to /RD Rise Hold Time	0		0		0		
15	ThIA(PC)	/INTACK to PCLK Rise Hold Time	38		30		15		
16	TsCEI(WR)	/CE Low to /WR Fall Setup Time	0		0		0		
17	ThCE(WR)	/CE to /WR Rise Hold Time	0		0		0		
18	TsCEh(WR)	/CE High to /WR Fall Setup Time	58		50		30		
19	TsCEI(RD)	/CE Low to /RD Fall Setup Time	0		0		0		[1]
20	ThCE(RD)	/CE to /RD Rise Hold Time	0		0		0		[1]
21	TsCEh(RD)	/CE High to /RD Fall Setup Time	58		50		30		[1]
22	TwRDI	/RD Low Width	145		125		70		[1,8]
23	TdRD(DRA)	/RD Fall to Read Data Active Delay	0		0		0		
24	TdRDr(DR)	/RD Rise to Data Not Valid Delay	0		0		0		
25	TdRDI(DR)	/RD Fall to Read Data Valid Delay		135		120		70	
26	TdRD(DRz)	/RD Rise to Read Data Float Delay		38		35		30	
27	TdA(DR)	Addr to Read Data Valid Delay		210		160		100	
28	TwWRI	/WR Low Width	145		125		75		
29	TdWR(DW)	/WR Fall to Write Data Valid Delay		35		35		20	
30	ThDW(WR)	Write Data to /WR Rise Hold Time	0		0		0		
31	TdWR(W)	/WR Fall to Wait Valid Delay		168		100		50	[4]
32	TdRD(W)	/RD Fall to Wait Valid Delay		168		100		50	[4]
33	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		168		120		70	
34	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		168		120		70	[6]
35a	TdWRr(REQ)	/WR Fall to /DTR//REQ Not Valid		4TcPc		4TcPc		4TcPc	
35b	TdWRr(REQ)	/WR Fall to /DTR//REQ Not Valid		168		100		70	[6]
36	TdRDr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		N/A		N/A		N/A	
37	TdPC(INT)	PCLK Fall to /INT Valid Delay		500		320		175	
38	TdIAi(RD)	/INTACK to /RD Fall (Ack) Delay	145		90		50		[5]
39	TwRDA	/RD (Acknowledge) Width	145		125		75		
40	TdRDA(DR)	/RD Fall(Ack) to Read Data Valid Delay	135		120		70		
41	TsIEI(RDA)	IEI to /RD Fall (Ack) Setup Time	95		80		50		
42	ThIEI(RDA)	IEI to /RD Rise (Ack) Hold Time	0		0		0		
43	TdIEI(IEO)	IEI to IEO Delay Time		95		80		45	
44	TdPC(IEO)	PCLK Rise to IEO Delay		195		175		80	
45	TdRDA(INT)	/RD Fall to /INT Inactive Delay		480		320		200	[4]
46	TdRD(WRQ)	/RD Rise to /WR Fall Delay for No Reset	15		15		10		
47	TdWRQ(RD)	/WR Rise to /RD Fall Delay for No Reset	15		15		10		
48	TwRES	/WR and /RD Low for Reset	145		100		75		
49a	Trc	Valid Access Recovery Time	3.5TcPc		3.5TcPc		3.5TcPc		[3]
49b	Trci	/RD or /WR Fall to PC Fall Setup Time	0		0		0		[7]

Notes:

[1] Parameter does not apply to Interrupt Acknowledge transactions.

[3] Parameter applies only between transactions involving the Z85C30 SL1480, if WR/RD falling edge is synchronized to PCLK falling edge, then TrC=3TcPc.

[4] Open-drain output, measured with open-drain test load.

[5] Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain. TsIEI(RDA) for the SCC and TdIEI(IEO) for each device separating them in the daisy chain.

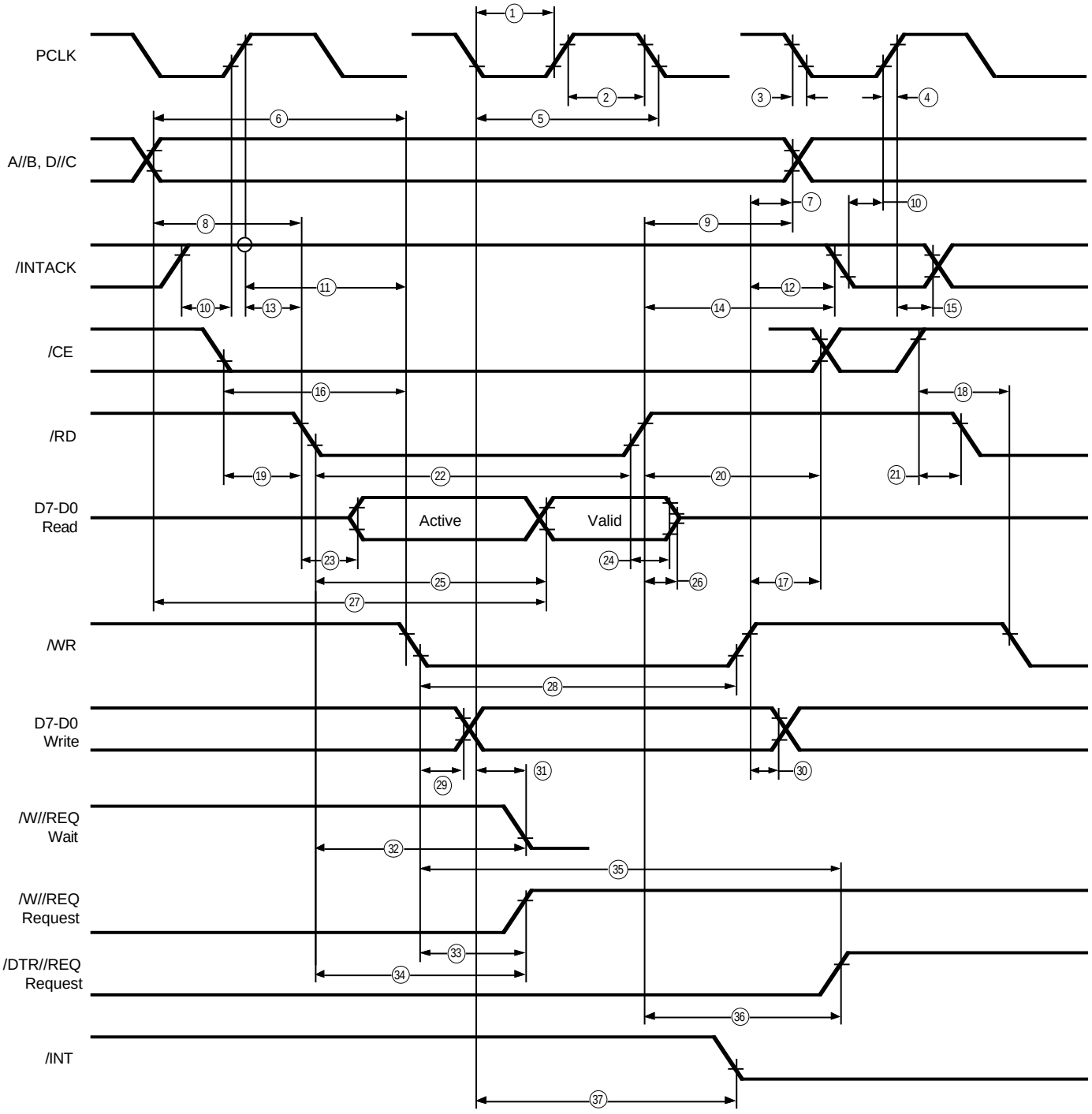
[6] Parameter applies to enhanced Request mode only (WR7' D4=1)

[7] This specification is only applicable when Valid Access Recovery Time is less than 3.5 PCLK.

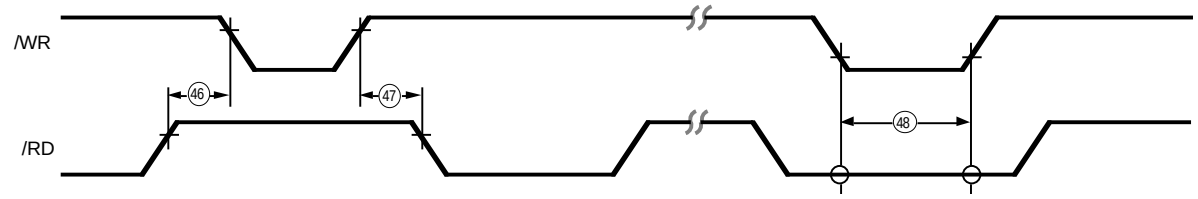
[8] The maximum for this spec. is 2TcPC. If there is >10ns setup time between the falling edge of /RD and the rising edge of PCLK, the second byte of Rx data will appear on the data bus after the falling edge of the second PCLK cycle; otherwise, the second byte of the Rx data will appear on the data after the third PCLK cycle.

AC CHARACTERISTICS

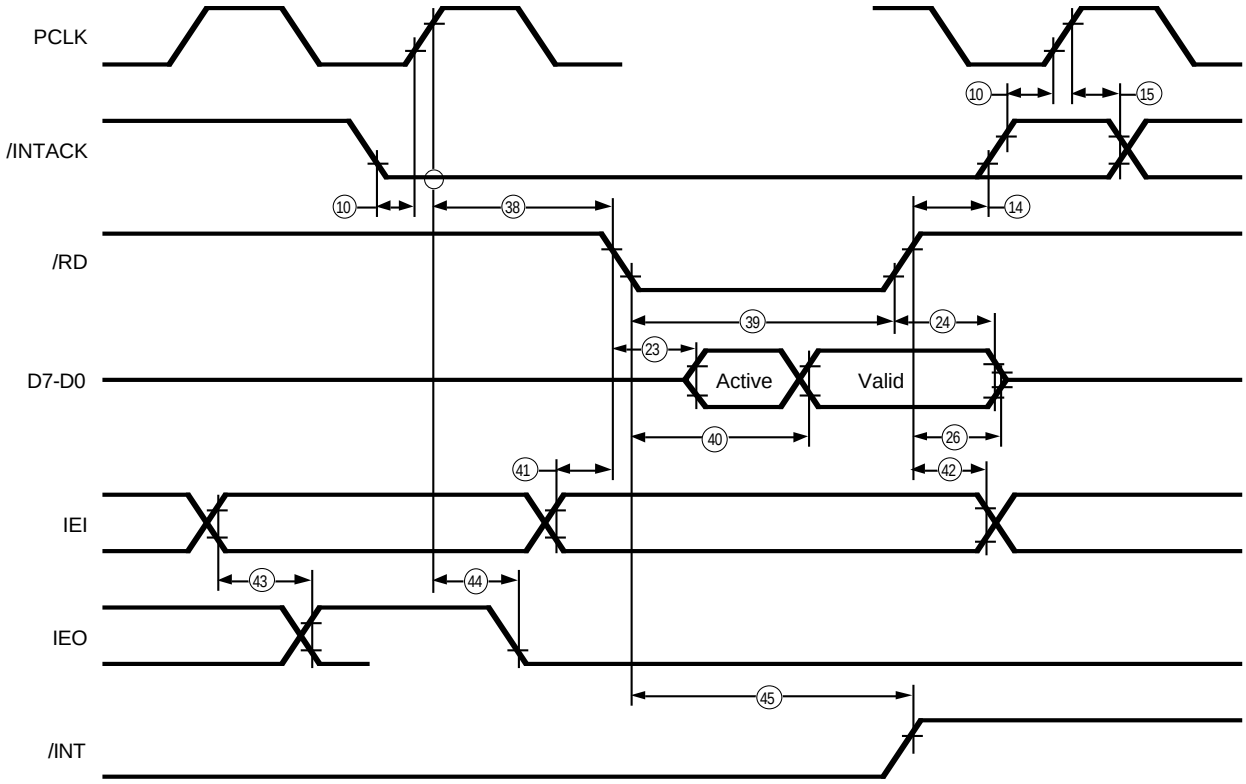
Z85C30 Read and Write Timing Diagram



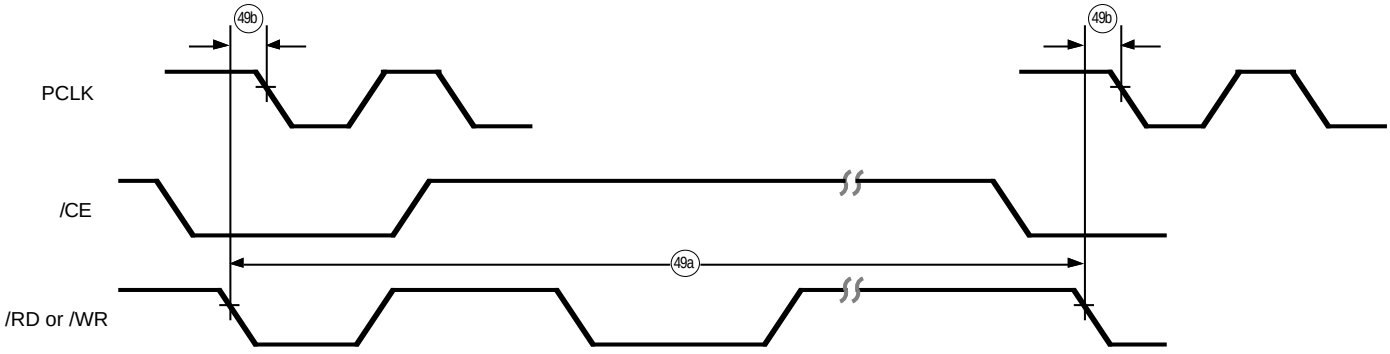
Z85C30 Read and Write Timing Diagram



Reset Timing Diagram



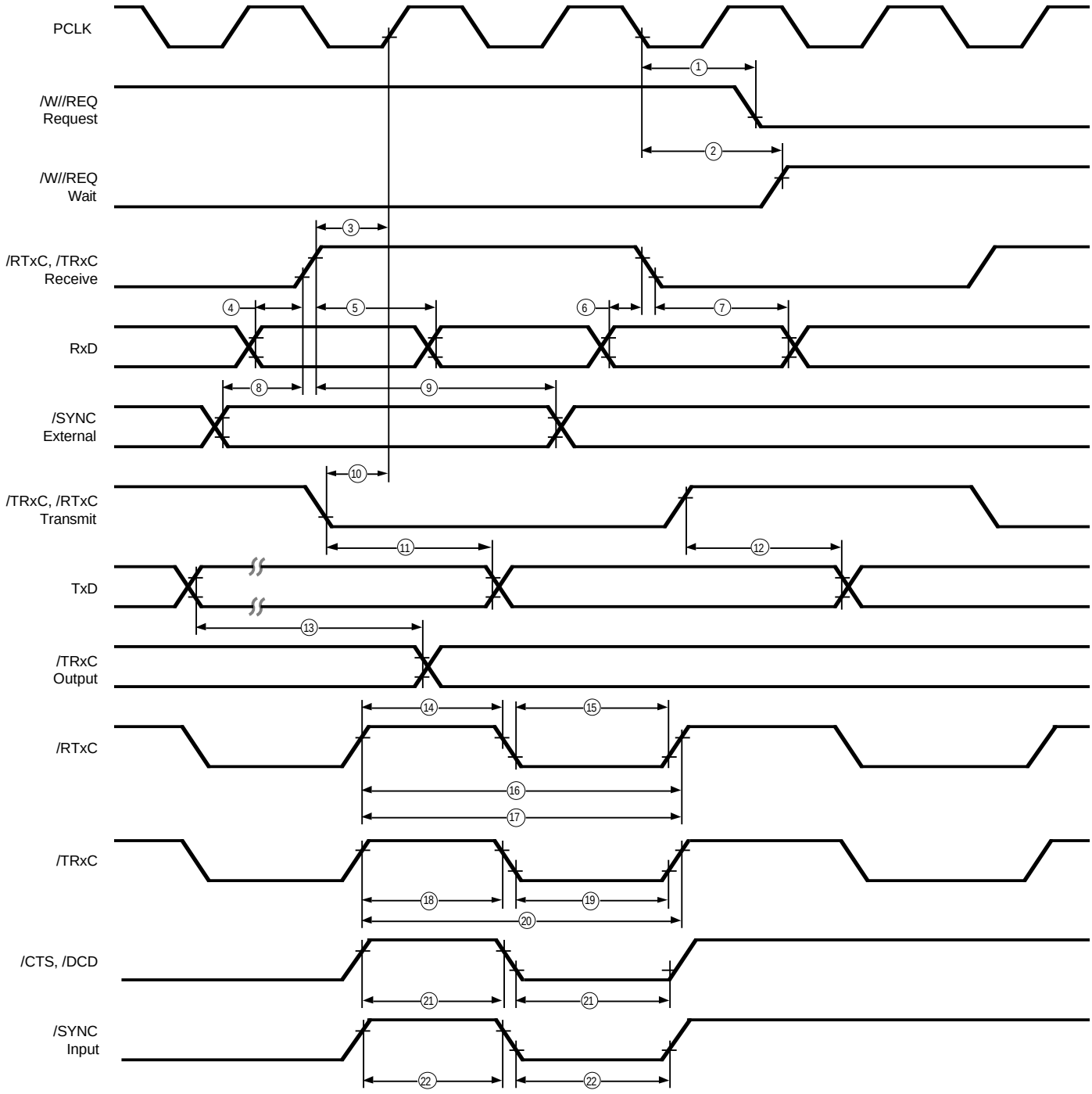
Interrupt Acknowledge Timing Diagram



Cycle Timing Diagram

AC CHARACTERISTICS

Z85C30 General Timing Diagram



Z85C30 SL1651 General Timing Diagram

AC CHARACTERISTICS

Z85C30 General Timing Table

No	Symbol	Parameter	8.5 MHz Min	8.5 MHz Max	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes
1	TdPC(REQ)	/PCLK to W/REQ Valid		250		150		80	
2	TdPC(W)	/PCLK to Wait Inactive		350		250		180	
3	TsRXC(PC)	/RxC to /PCLK Setup Time	N/A		N/A		N/A		[1,4]
4	TsRXD(RXCr)	RxD to /RxC Setup Time		0		0		0	[1]
5	ThRXD(RxCr)	RxD to /RXC Hold Time	150		125		50		[1]
6	TsRXD(RXCf)	RxD to /RXC Setup Time	0		0		0		[1,5]
7	ThRXD(RXCf)	RXD to /RXC Hold Time	150		125		50		[1,5]
8	TsSY(RXC)	/SYNC to /RxC Setup Time	-200		-150		-100		[1]
9	ThSY(RXC)	/SYNC to/RXC Hold Time	5TcPc		5TcPc		5TcPc		[1]
10	TsTXC(PC)	/TxC to /PCLK Setup Time	N/A		N/A		N/A		[2,8]
11	TdTXCf(TXD)	/TxC to TxD Delay		200		150		80	[2]
12	TdTxCr(TXD)	/TxC to TxD Delay		200		150		80	[2,5]
13	TdTXD(TRX)	TxD to TRxC Delay		200		140		80	
14a	TwRTXh	RTxC High Width	150		120		80		[6]
14b	TwRTXh(E)	/RTxC High Width	50		40		15.6		[9]
15a	TwRTXl	TRxC Low Width	150		120		80		[6]
15b	TwRTXl(E)	/RTxC Low Width	50		40		15.6		[9]
16a	TcRTX	RTxC Cycle Time	488		400		244		[6,7]
16b	TcRTX(E)	/RTxC Cycle Time	125		100		31.25		[9]
17	TcRTXX	Crystal Osc. Period	125	1000	100	1000	62	1000	[3]
18	TwTRXh	/TRxC High Width	150		120		180		[6]
19	TwTRXl	/TRxC Low Width	150		120		80		[6]
20	TcTRX	/TRxC Cycle Time	488		400		244		[6,7]
21	TwEXT	/DCD or /CTS Pulse Width	200		120		70		
22	TwSY	/SYNC Pulse Width	200		120		70		

Notes:

[1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.

[2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.

[3] Both /RTxC and /SYNC have 30 pF capacitors to ground connected to them.

[4] Synchronization of RxC to PCLK is eliminated in divide by four operation.

[5] Parameter applies only to FM encoding/decoding.

[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.

[7] The maximum receive or transmit data rate is 1/4 PCLK.

[8] External PCLK to /RTxC or /RTxC synchronization requirement eliminated for PCLK divide-by-four operation.

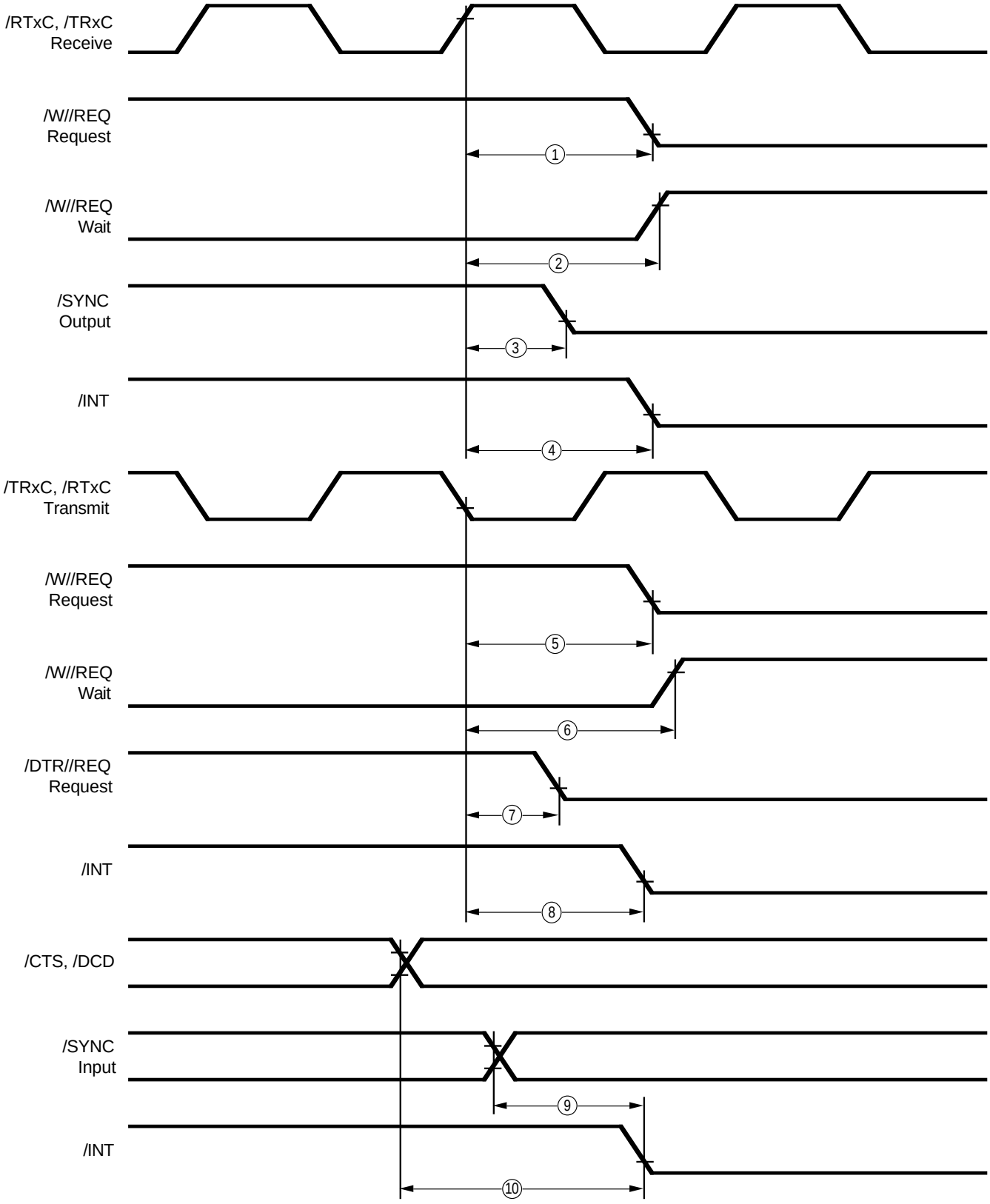
/TRxC and /RTxC rise and fall times are identical to PCLK. Reference timing specs TfPC and TrPC.

Tx and Rx input clock slew rates should be kept to a maximum of 30 nsec. All parameters related to input CLK edges should be referenced at the point at which the transition begins or ends, whichever is worst case.

[9] ENHANCED FEATURE - /RTxC used as input to internal DPLL only.

AC CHARACTERISTICS

Z85C30 System Timing Diagram



Z85C30 SL1651 System Timing

AC CHARACTERISTICS

Z85C30 System Timing Table

No	Symbol	Parameter	8.5 MHz Min	8.5 MHz Max	10 MHz Min	10 MHz Max	16 MHz Min	16 MHz Max	Notes
1	TdRXC(REQ)	/RxC High to /W//REQ Valid	8	12	8	12	8	12	[2,5]
2	TdRXC(W)	/RxC High to Wait Inactive	8	14	8	14	8	14	[1,2,5]
3	TdRdXC(SY)	/RxC High to /SYNC Valid	4	7	4	7	4	7	[2,5]
4	TsRXC(INT)	/RxC High to INT Valid	10	16	10	16	10	16	[1,2,5]
5	TdTXC(REQ)	/TxC Low to /W//REQ Valid	5	8	5	8	5	8	[3]
6	TdTXC(W)	/TxC Low to Wait Inactive	5	11	5	11	5	11	[1,3]
7a	TdTXC(DRQ)	/TxC Low to /DTR//REQ Valid	4	7	4	7	4	7	[3]
7b	TdTXC(EDRQ)	/TxC Low to /DTR//REQ Valid	5	8	5	8	5	8	[3,4]
8	TdTXC(INT)	/TxC Low to /INT Valid	6	10	6	10	6	10	[1,3]
9	TdSY(INT)	SYNC to INT Valid	2	6	2	6	2	6	[1]
10	TdEXT(INT)	/DCD or /CTS to /INT Valid	2	6	2	6	2	6	[1]

Notes:
[1] Open drain-output, measured with open-drain test load.
[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[4] Parameter applies to Enhanced Request mode only.

ERRATA

Problem:

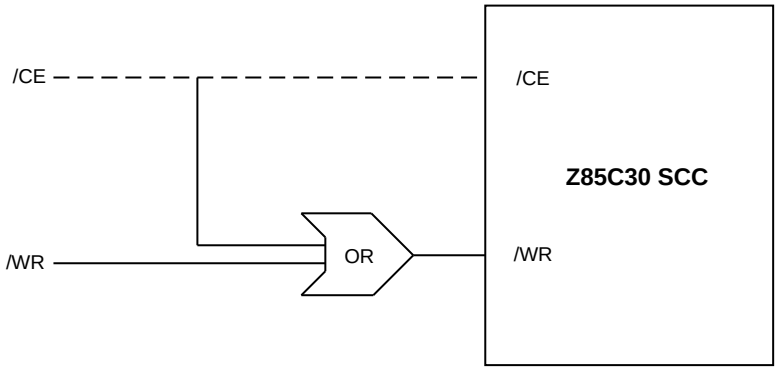
The SCC may have invalid data written into its registers/ FIFO if parameter #49 (Trc, Valid Access Recovery Time) is violated. If the CPU does another write operation to SCC or any other device during the 3 to 3.5 PCLK time period required by the SCC to complete its internal WRITE, the SCC may write incorrect data to its internal registers/FIFO. It is possible to write incorrect data into the SCC when writing to other peripherals, since the SCC does not qualify the write strobe (/WR) with chip enable (/CE). In most applications, PCLK is the same or faster than CPU clock and the CPU cannot do another read or write access in the recovery time required by the SCC, or the above will be a problem.

Workaround:

If PCLK is slower than the CPU clock than any extra non-SCC WRITEs during the valid access recovery time can be stopped by OR-gating the external /WR with /CE of the SCC. (The "/ " indicates an active low.)

As far as extra SCC WRITEs during the same valid access recovery time, there cannot be a workaround as this is a violation of parameter #49.

Note:
The following problem may occur also on a read cycle when access to another peripheral is attempted within the valid access recovery time of the SCC. Therefore, the same type of gating logic will need to be implemented for /CE and /RD also.



Workaround Example

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FAX 408 370-8056